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1125-CS

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U.S. Ser. No. 09/ 821,897

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

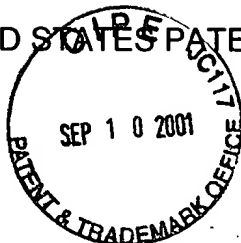
Applicant; Luo, Zheng

Serial No.: 09/821,897

Filed: 03/30/2001

Title: SYSTEM ON A CHIP WITH MULTIPLE POWER PLANES AND ASSOCIATE
POWER MANAGEMENT METHODS

Hon. Commissioner of Patents
Customer Service Center
Initial Patent Examination Division
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Sept 8, 2001
Date

ATTENTION TO THE OFFICIAL DRAFTSMAN
TRANSMITTAL OF FORMAL DRAWINGS

Transmitted herewith are is thirty-seven (37) sheets of formal drawings to be substituted for the drawings originally filed in connection with the above-identified application for patent.

Respectfully submitted,
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Attorney's Docket: 2836- P139US

By: [Signature]
James J. Murphy
Reg. No. 34,503

Date Sept. 7, 2001

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/821,897	03/30/2001	Luo Zheng	1125-CS

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CONFIRMATION NO. 8975

FORMALITIES LETTER



OC000000006434480

Date Mailed: 08/16/2001

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

This application has been accorded an Application Number and Filing Date. The application, however, is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a)

The required item(s) identified below must be timely submitted to avoid abandonment:

- **Substitute drawings in compliance with 37 CFR 1.84 because:**
 - **drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);**

A copy of this notice MUST be returned with the reply.

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PART 2 - COPY TO BE RETURNED WITH RESPONSE

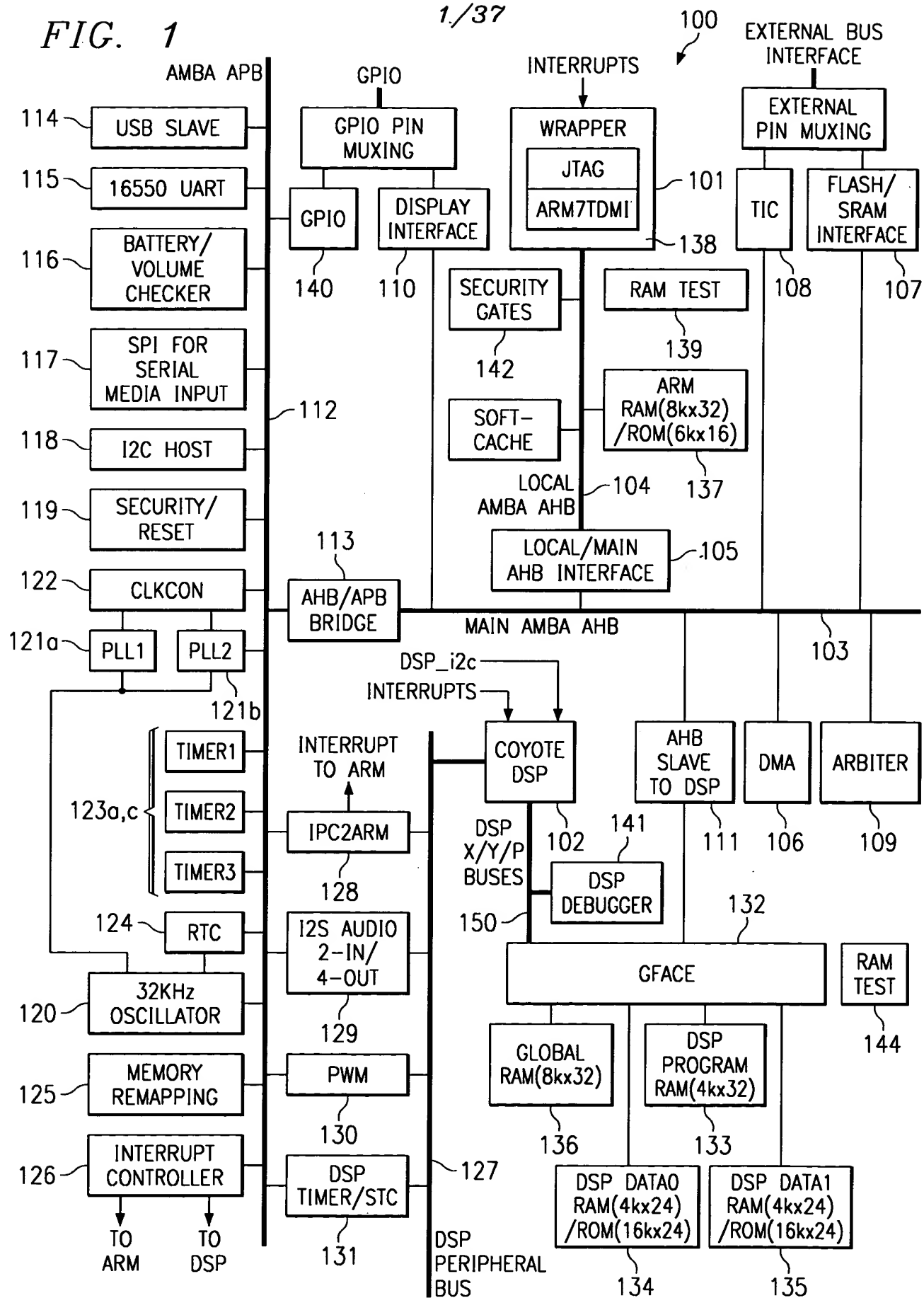
07/17/2001 BABRAHA1 00000041 05821897

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10.00 00

FIG. 1

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T00T60" 2007:001001

FIG. 2A

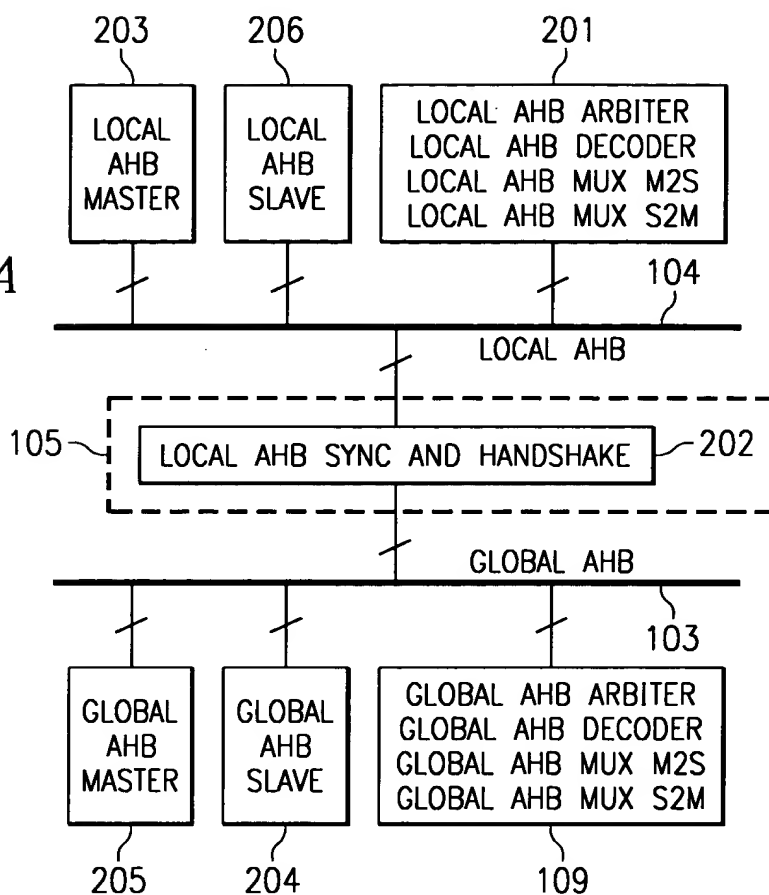


FIG. 3

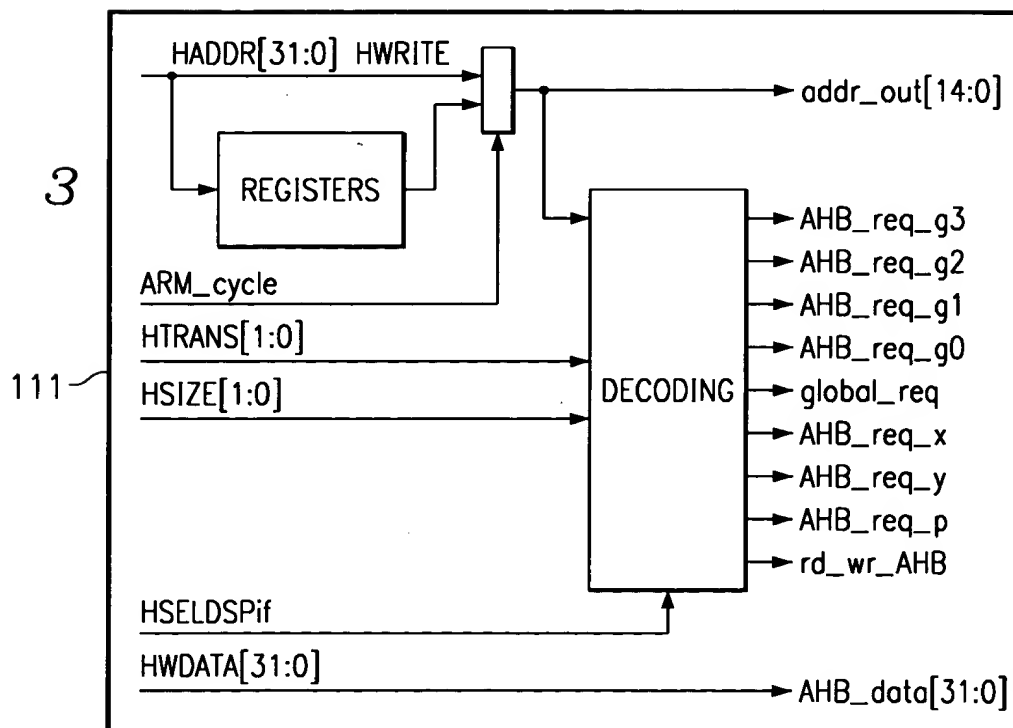


FIG. 2B

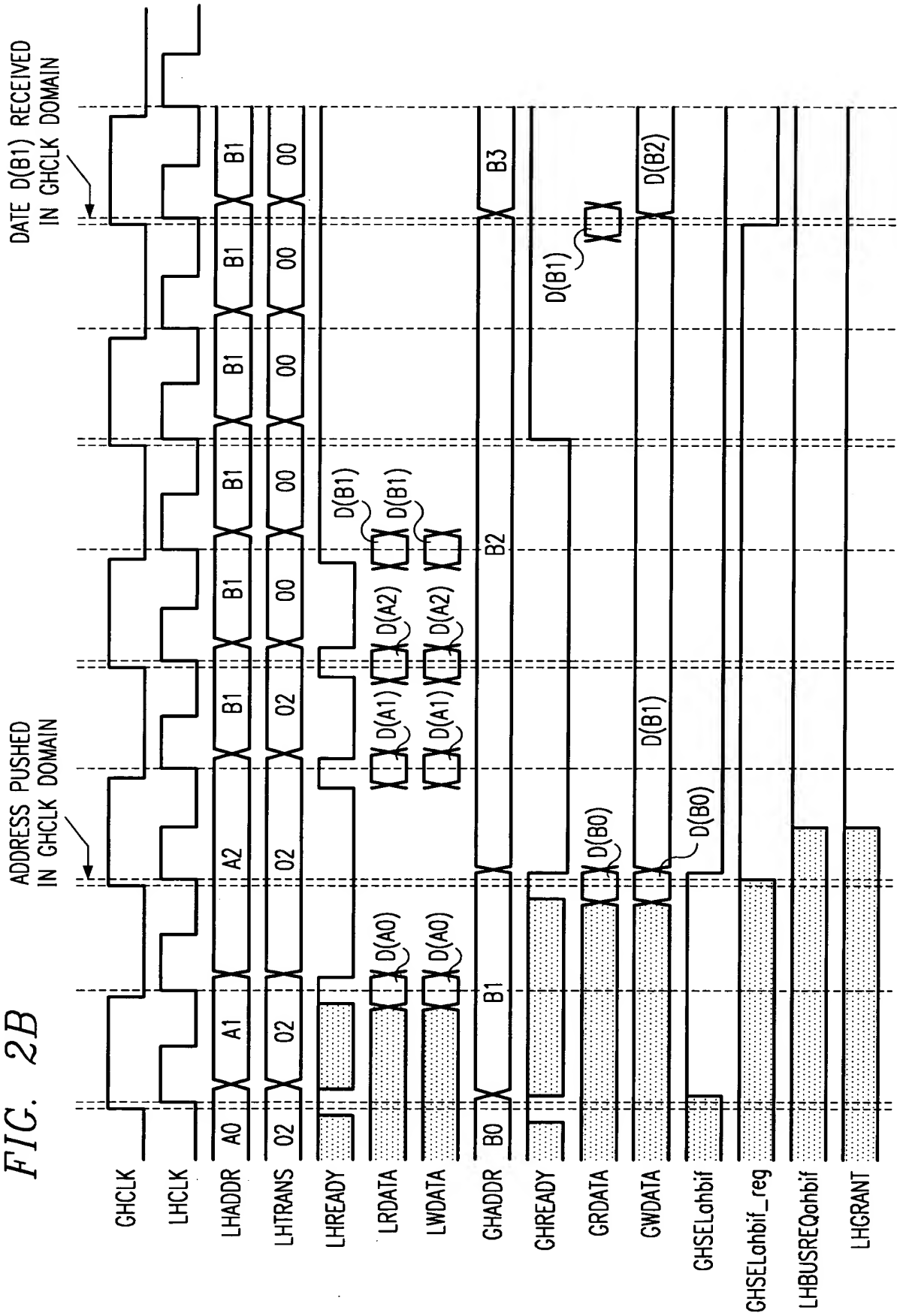
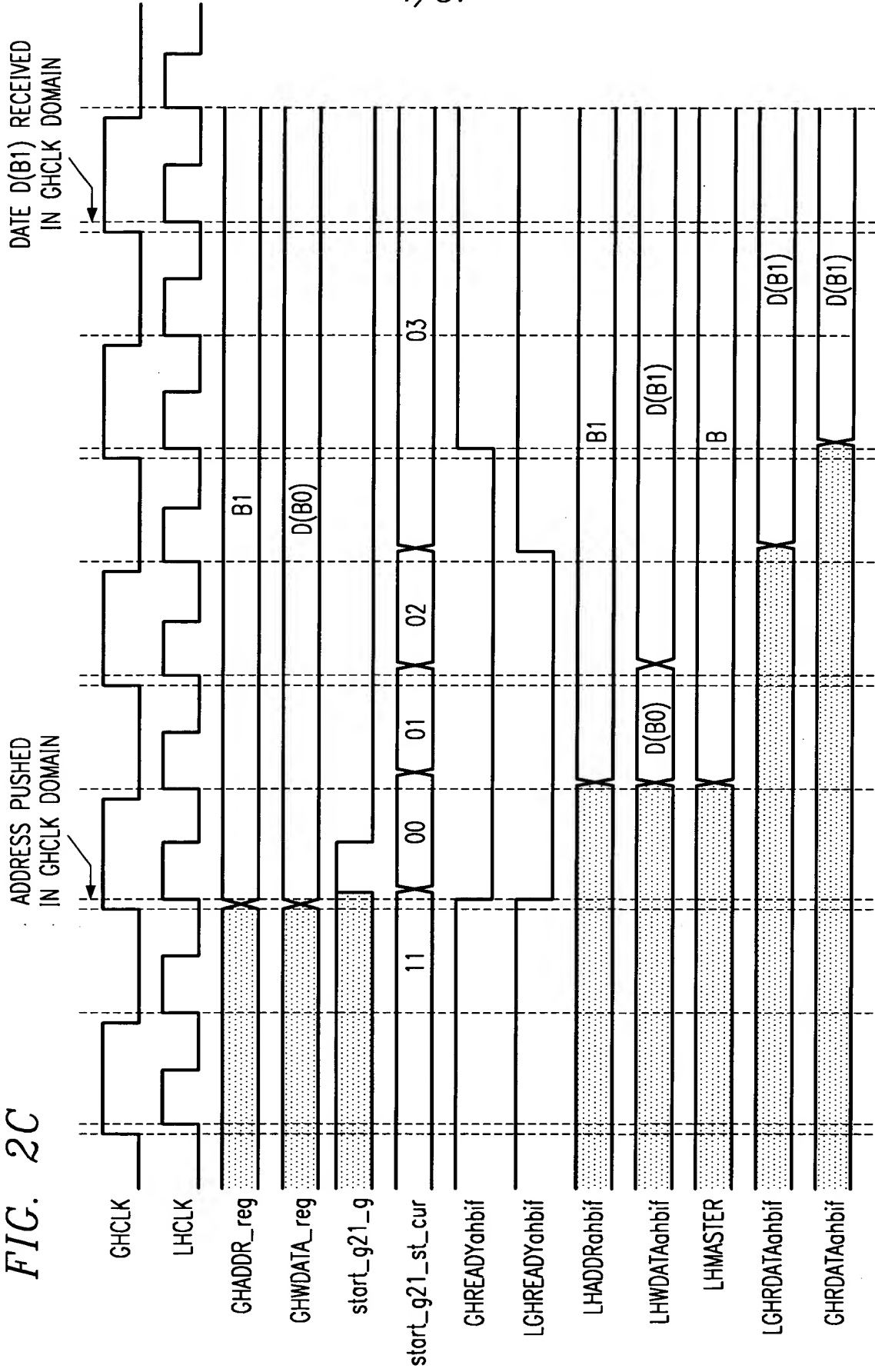
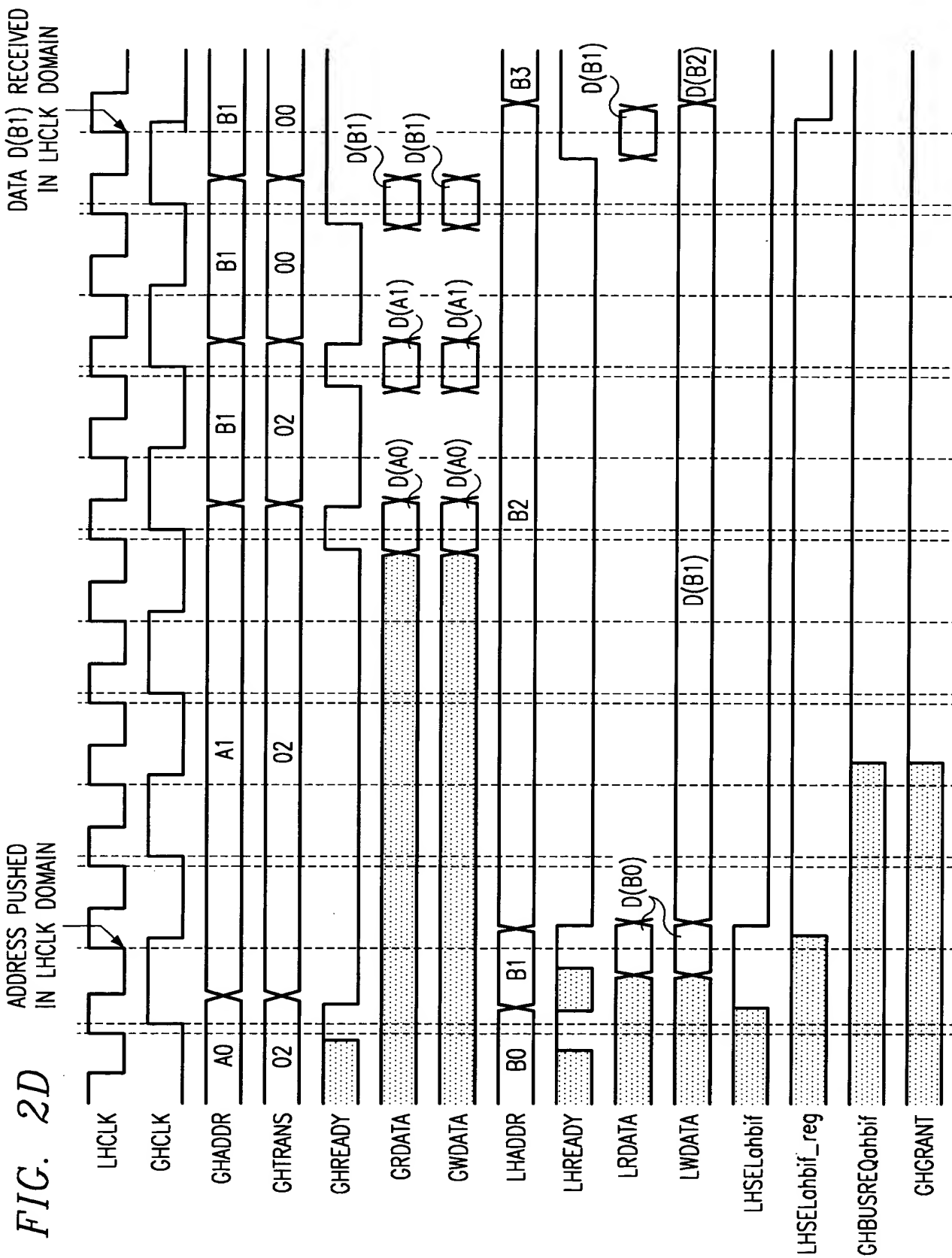
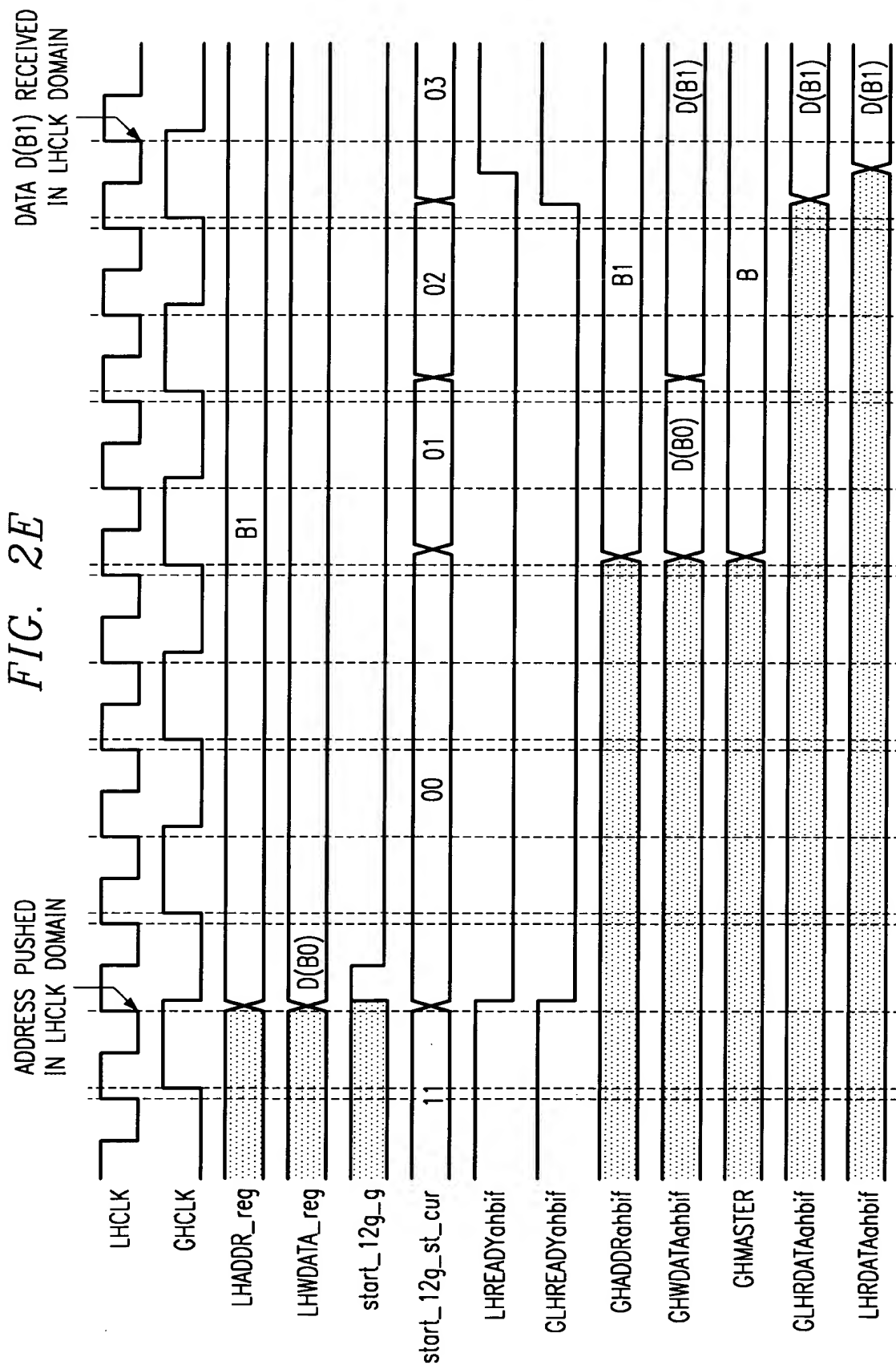


FIG. 2C







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FIG. 4A

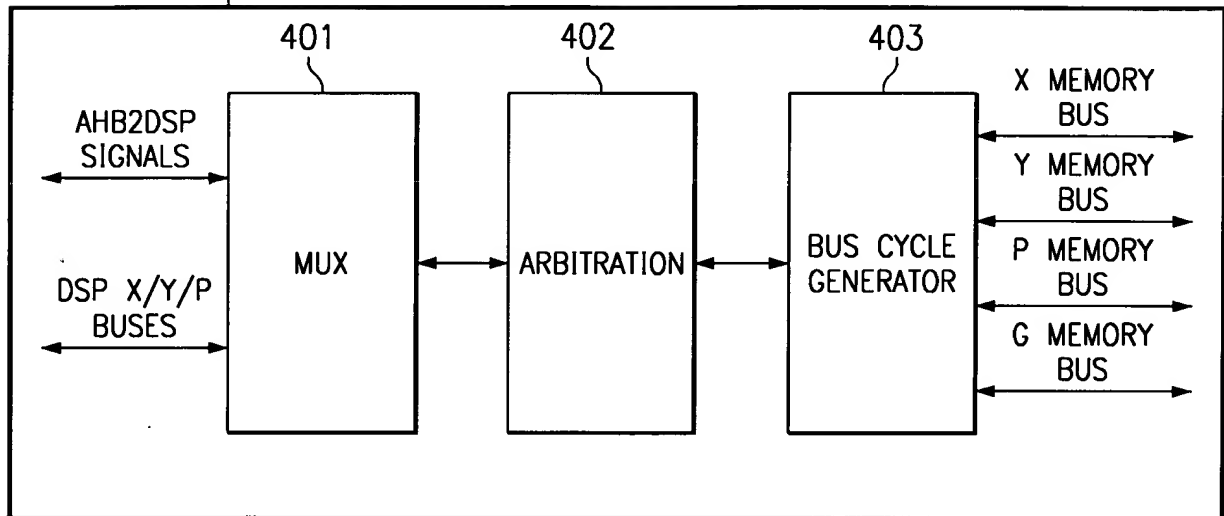
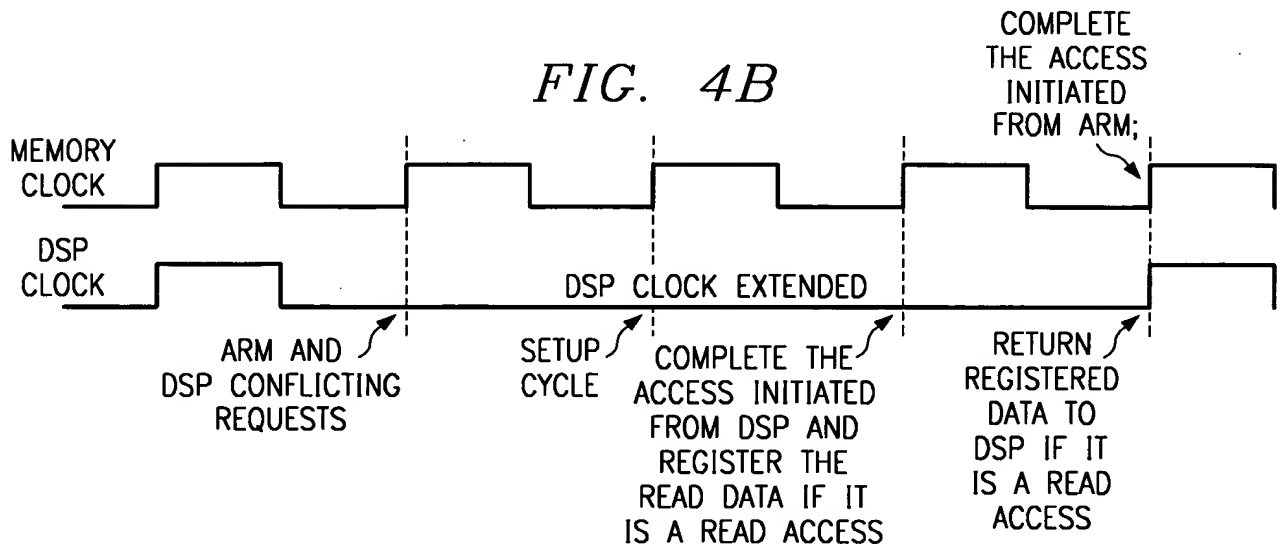
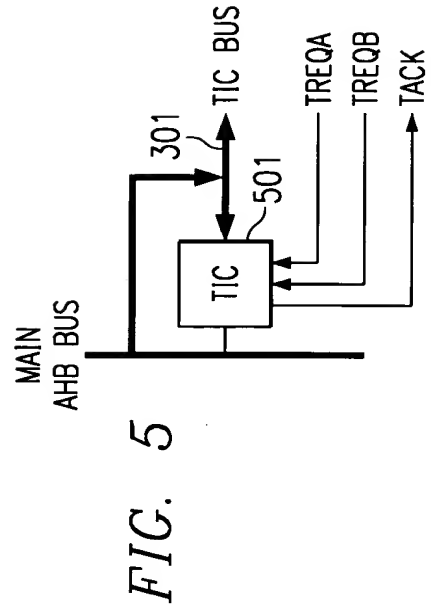
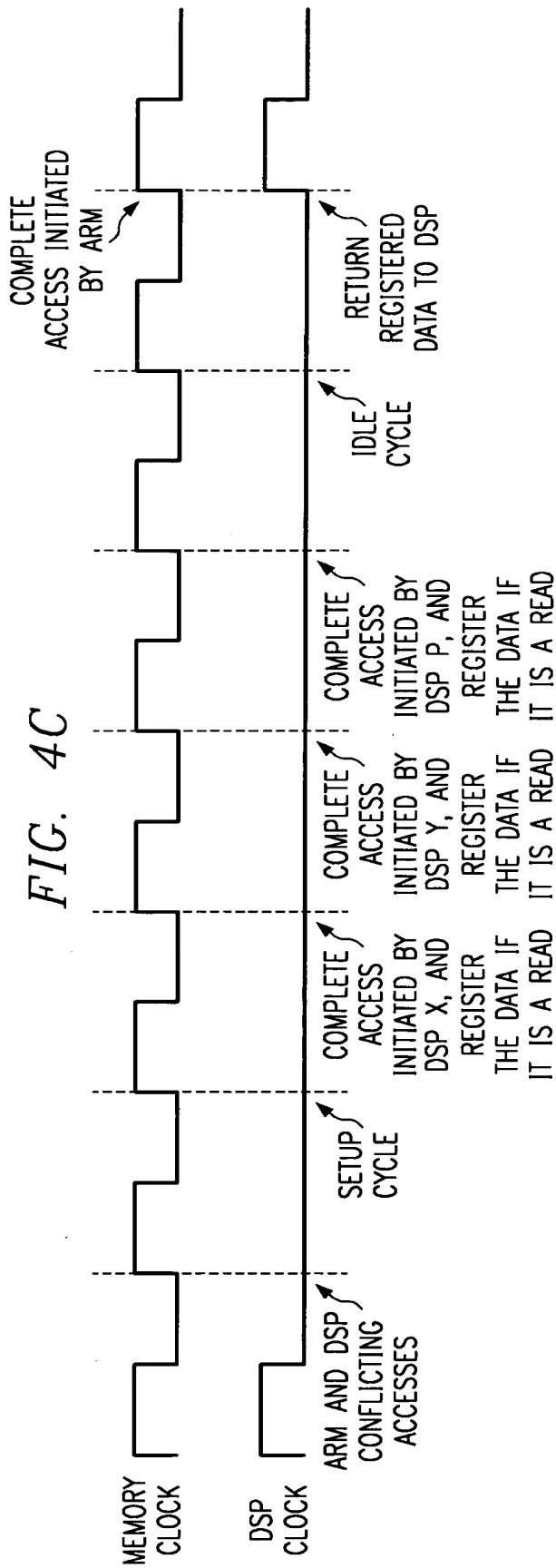


FIG. 4B





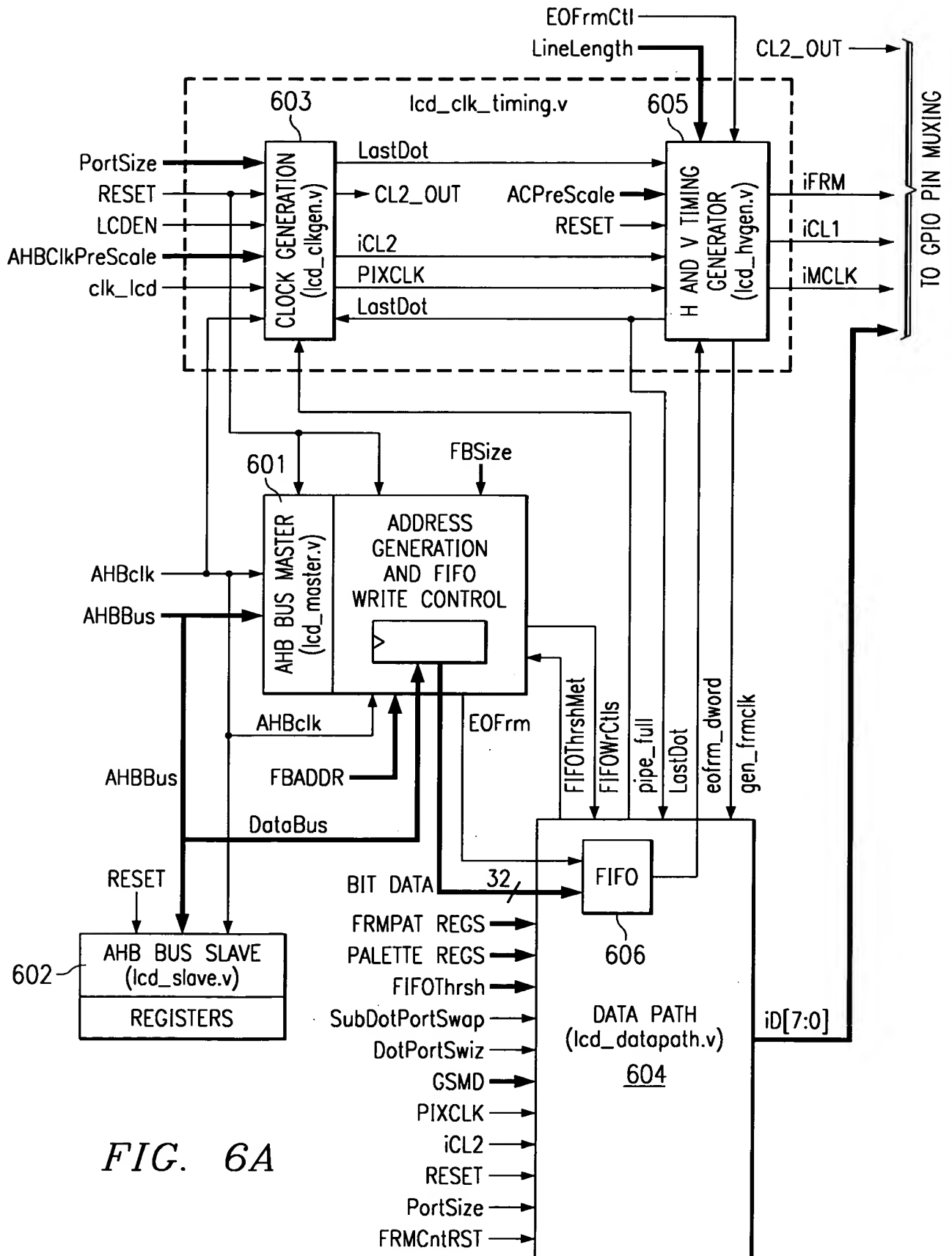


FIG. 6A

FIG. 6B

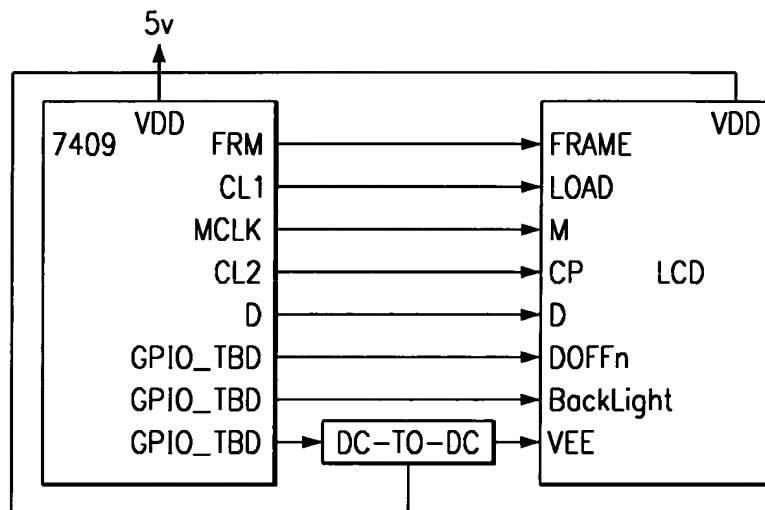
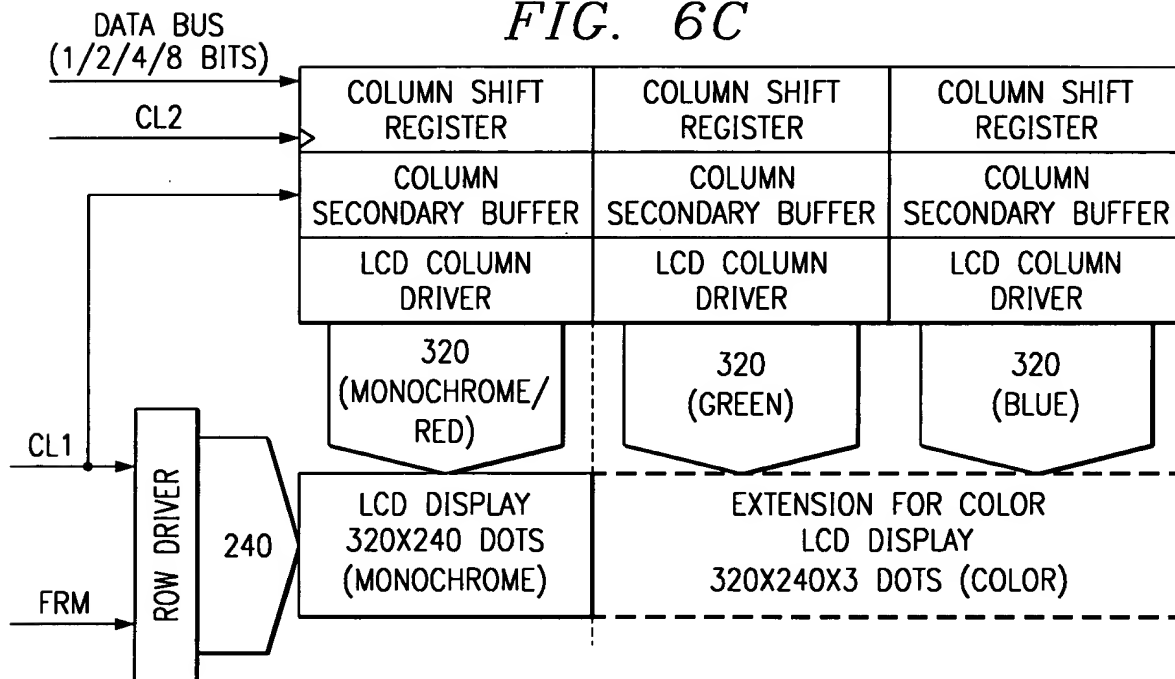
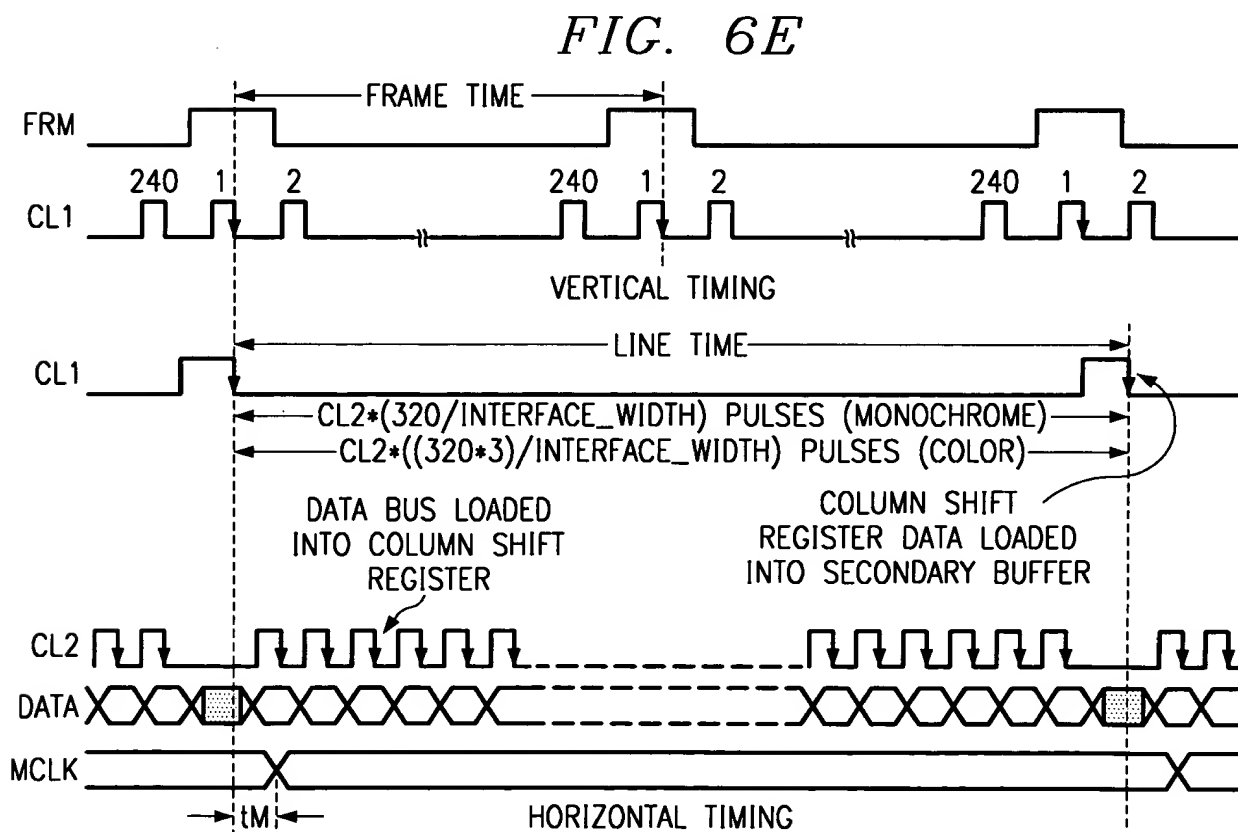
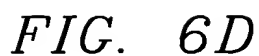


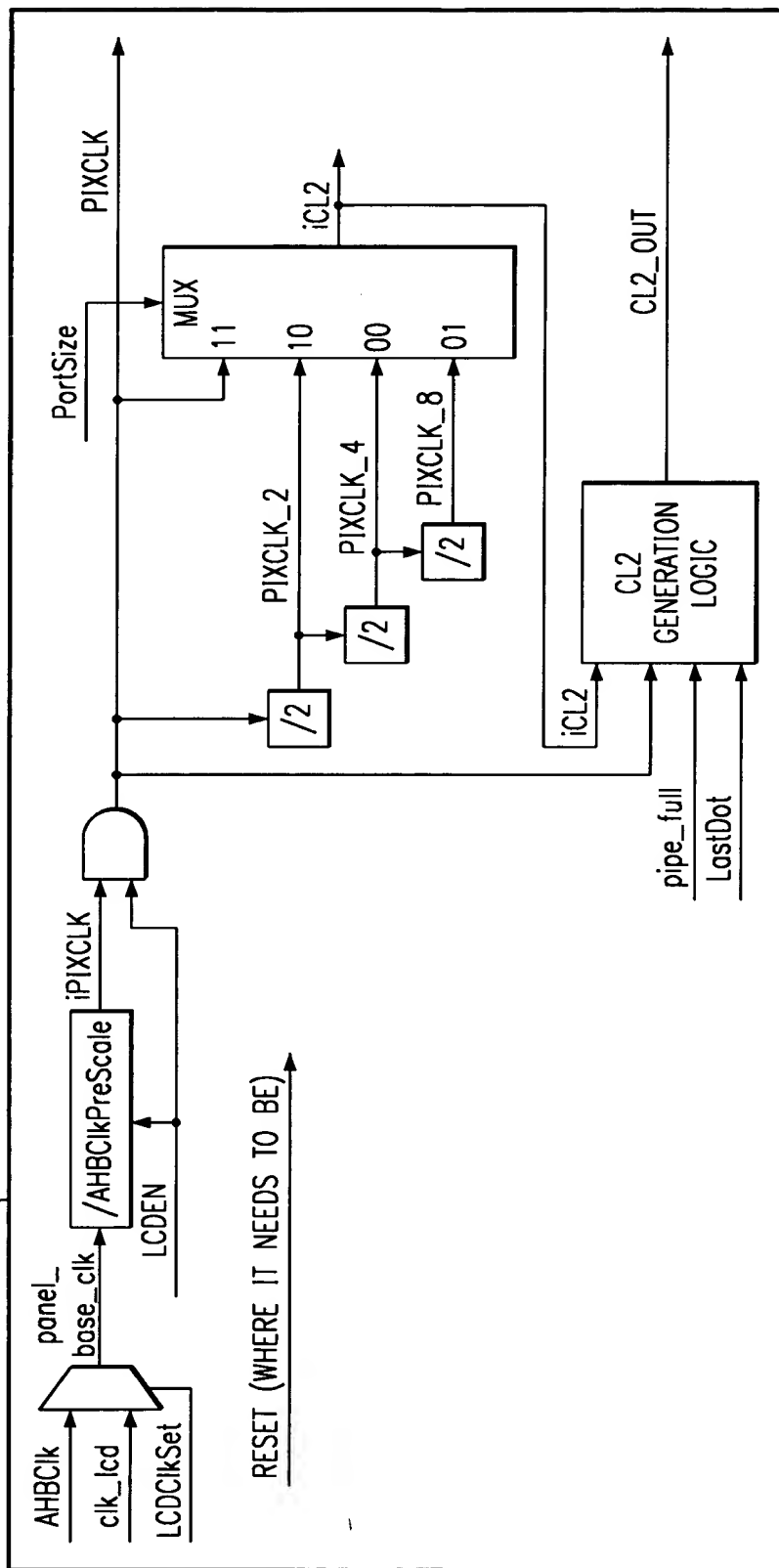
FIG. 6C





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FIG. 6C



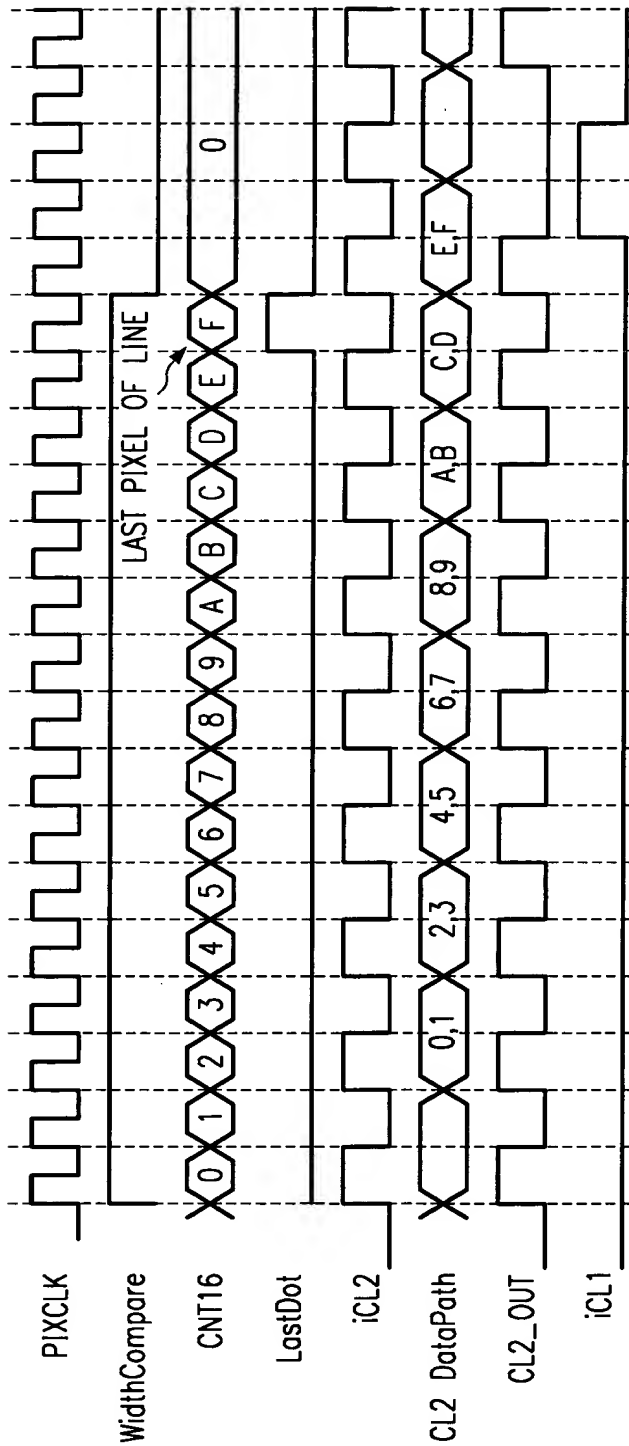


FIG. 6H

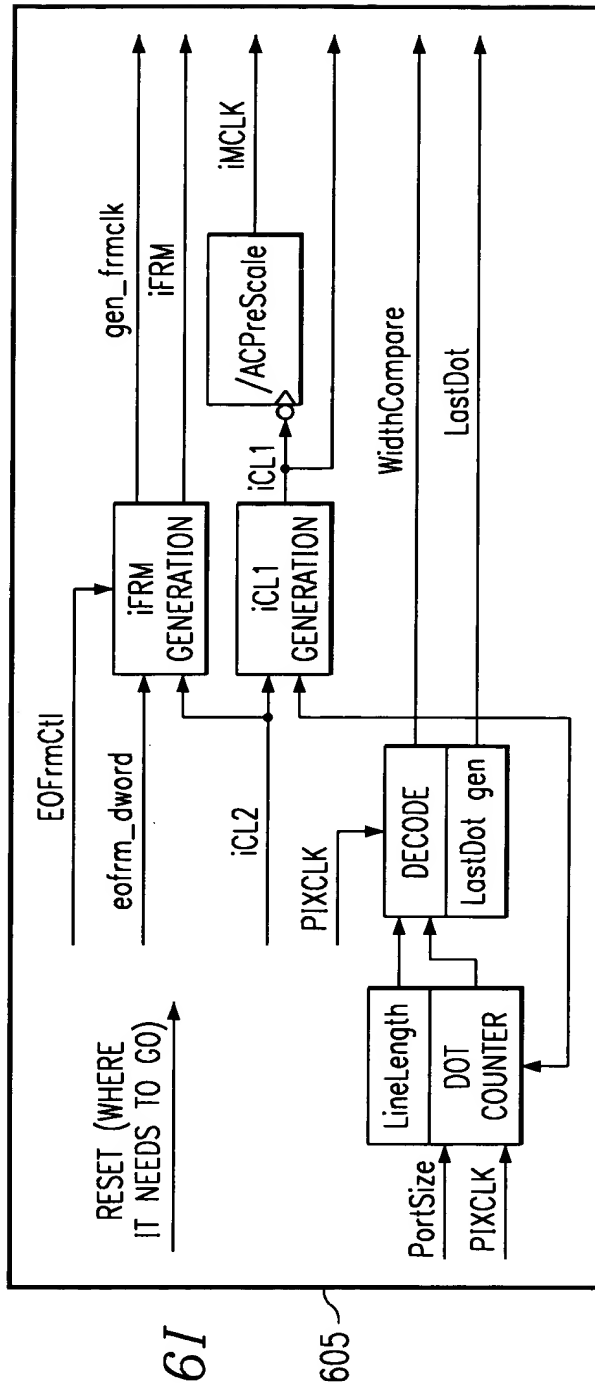


FIG. 6I

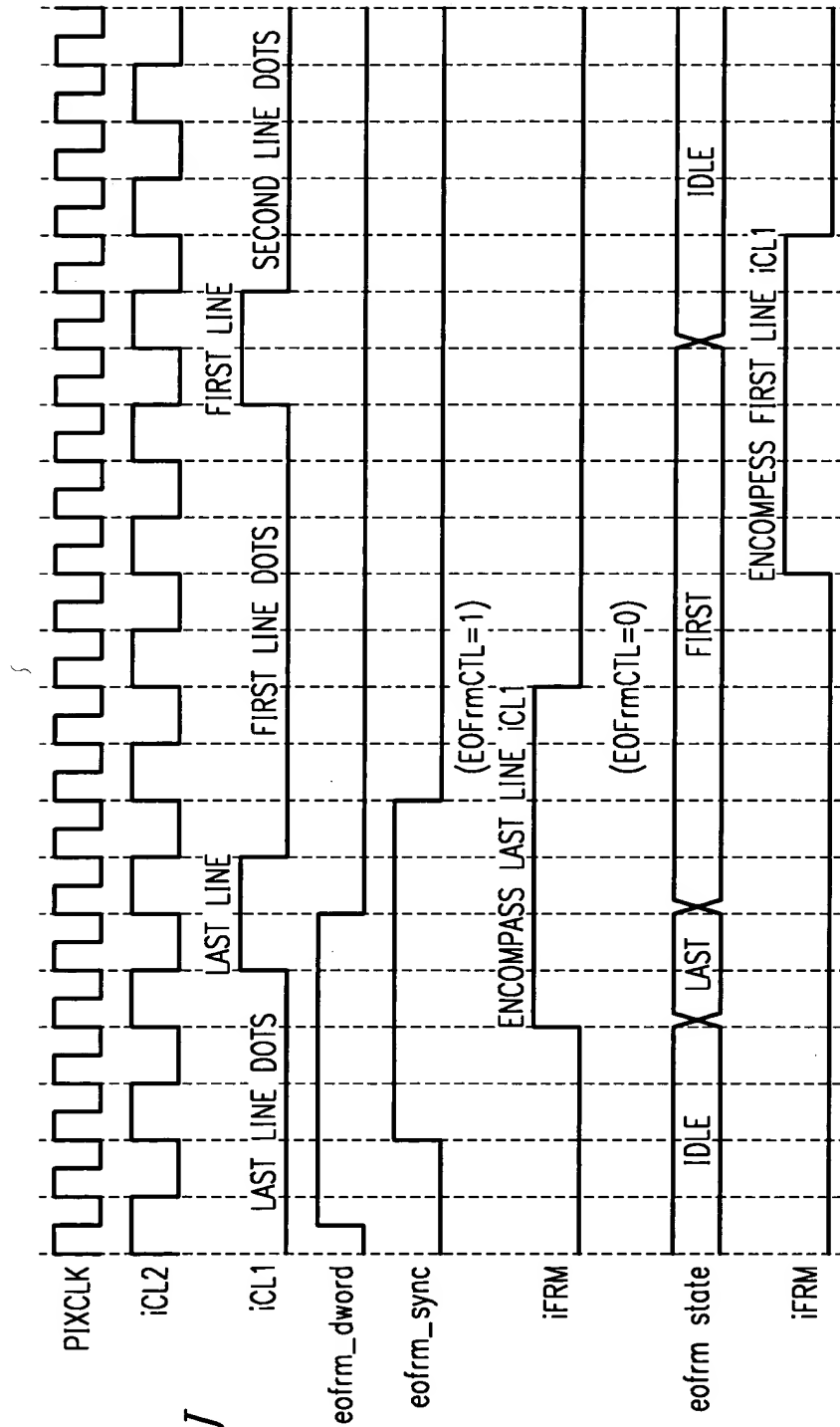


FIG. 6J

FIG. 6K

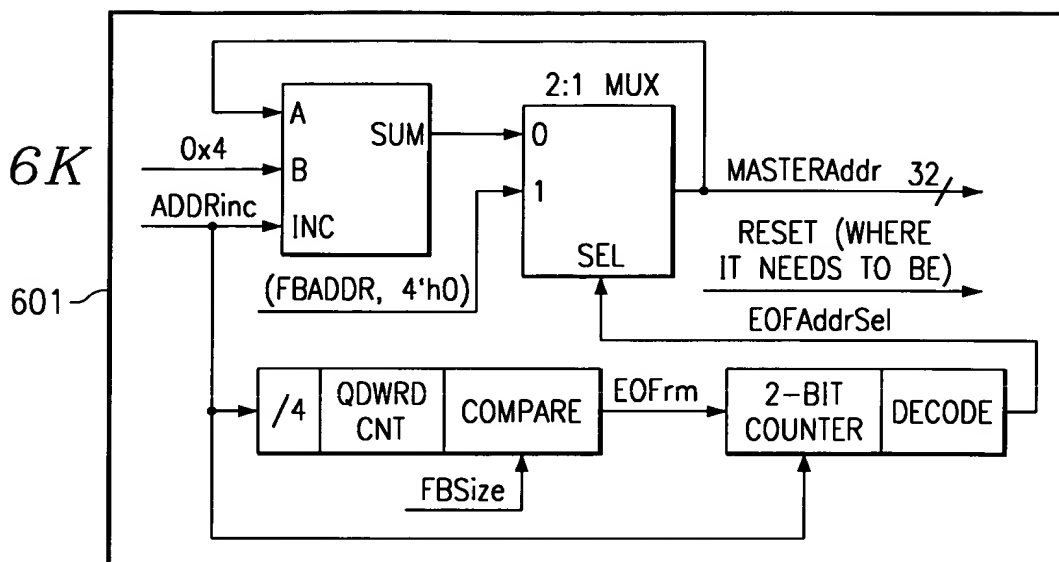


FIG. 17

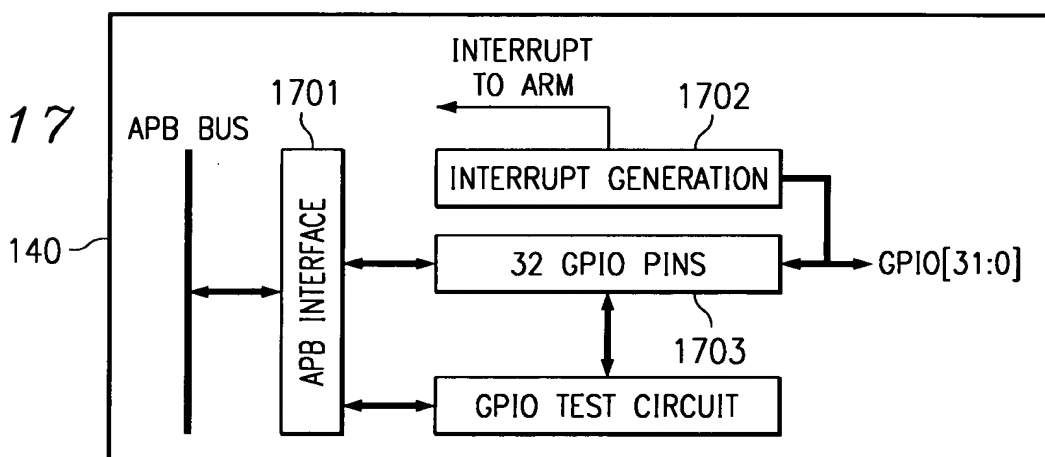
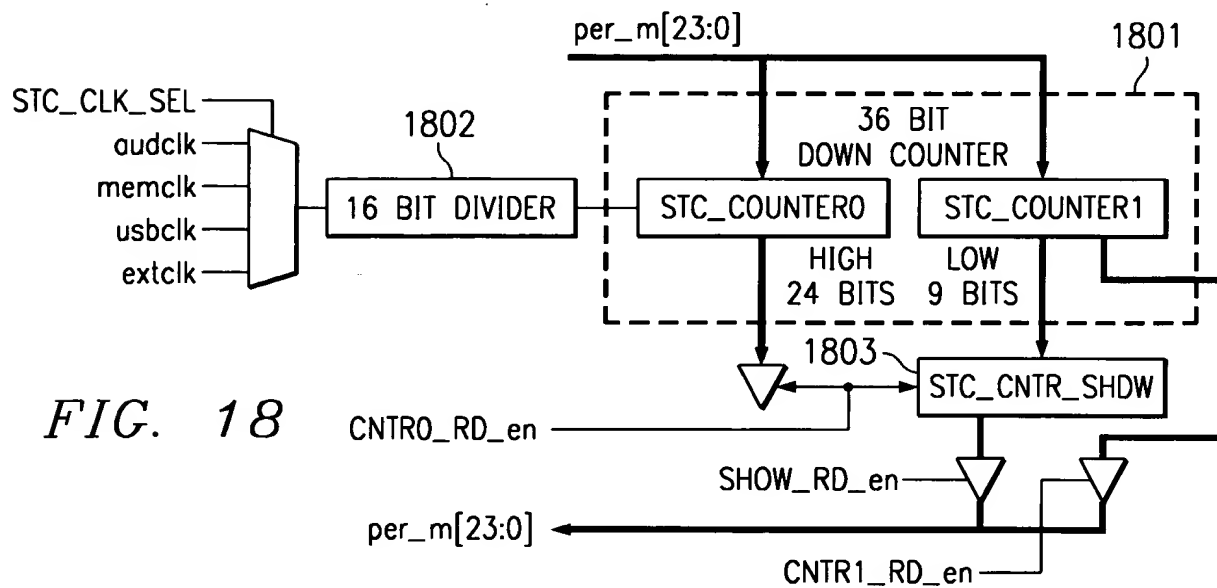


FIG. 18



CNTR0_RD_en

SHOW_RD_e

CNTR1_RD_en

4-BITS/PIXEL

FBADDR [31:0] 0 31
 G R B G R B G R B G R B G R B G R B
 [3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0][3:0]
 PIX8 PIX16 PIX32 PIX64
 NEXT LINE ADDRESS = FBADDR + ((LineLength*16)*(bite/pixel))/8 (LineLength*16) - 7

2-BITS/PIXEL

FBADDR [31:0] 0 31
 R B G R B G R B G R B G R B G R B G R
 [1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0][1:0]
 PIX16 PIX32 PIX64 PIX128
 NEXT LINE ADDRESS = FBADDR + ((LineLength*16)*(bite/pixel))/8 (LineLength*16) - 15

1-BIT/PIXEL

FBADDR [31:0] 0 31
 [0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0][0:0]
 PIX32 PIX64 PIX128 PIX256
 NEXT LINE ADDRESS = FBADDR + ((LineLength*16)*(bite/pixel))/8 (LineLength*16) - 31

FIG. 6M

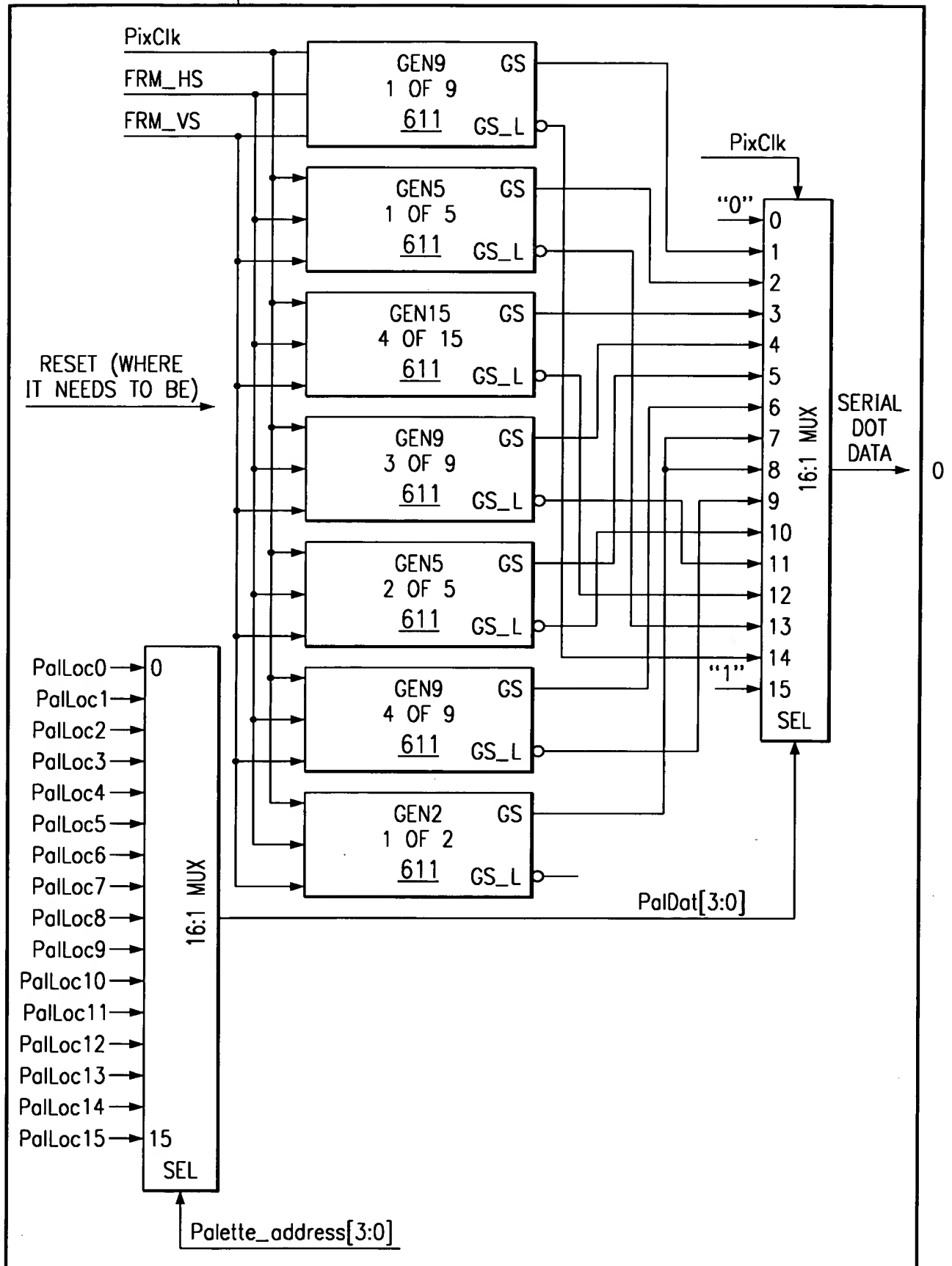


FIG. 6N

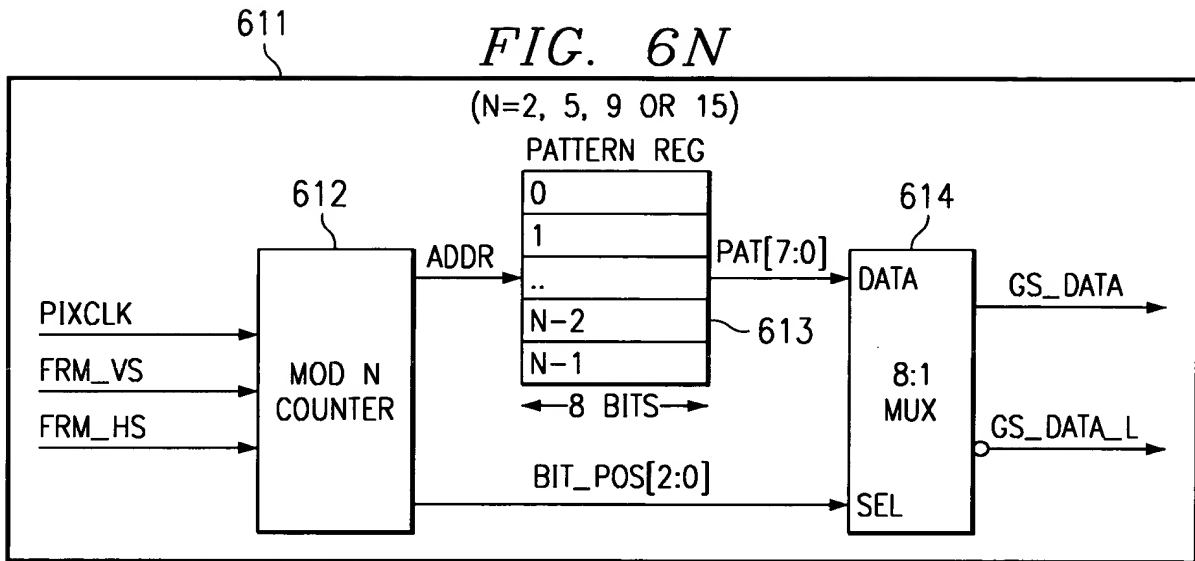


FIG. 60

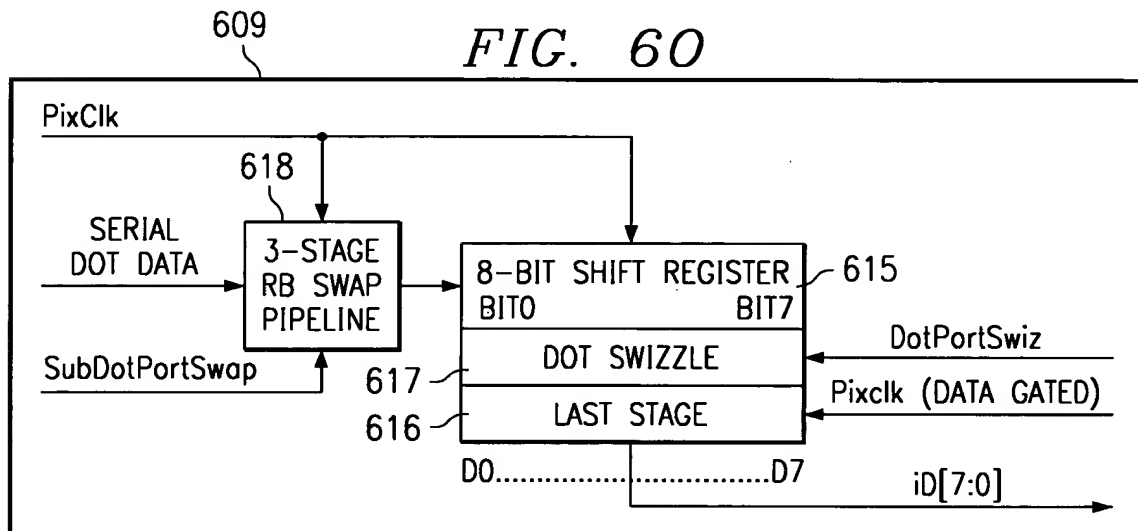


FIG. 6P

TIME (FROM THE SHIFT REGISTER POINT OF VIEW)

SubDotPortSwap=0

$$\{B_n G_n R_n\} \dots \{B_3 G_3 R_3\} \{B_2 G_2 R_2\} \{B_1 G_1 R_1\} \{B_0 G_0 R_0\}$$

SubDotPortSwap=1

FIG. 6R

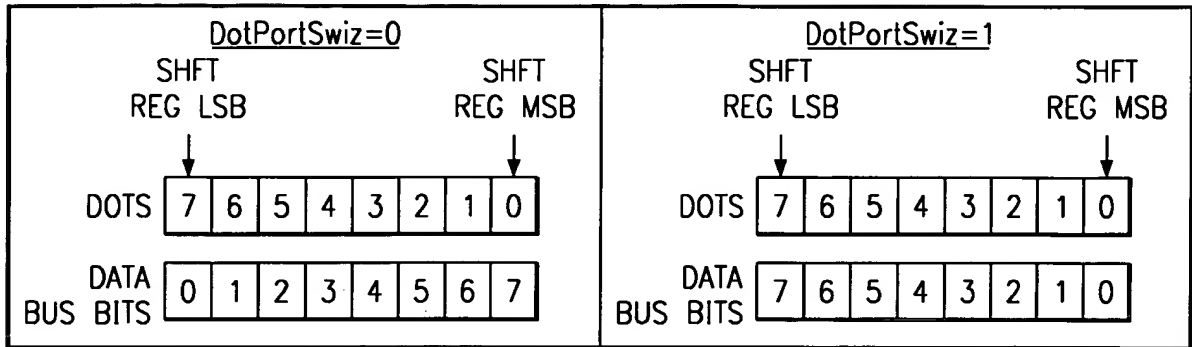


FIG. 6S

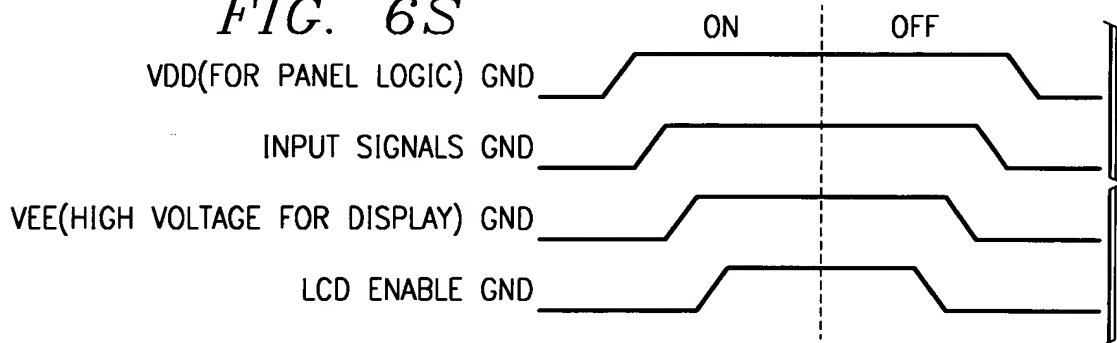
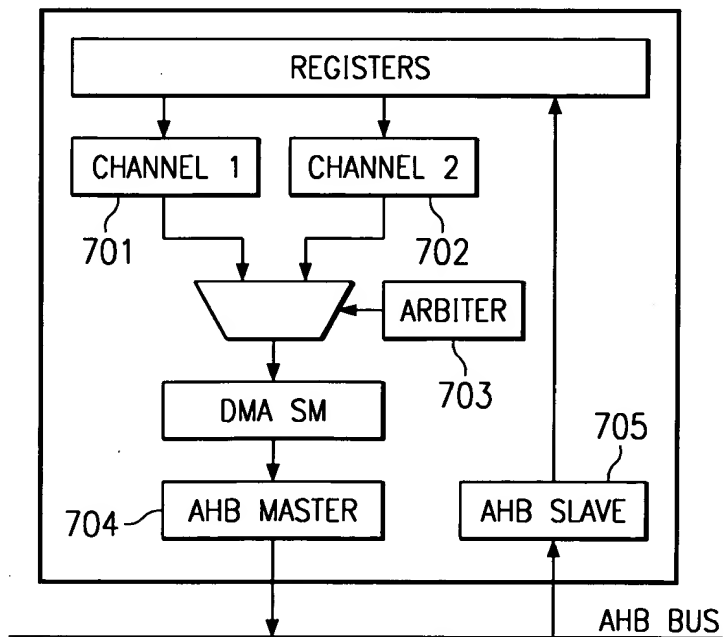


FIG. 7A



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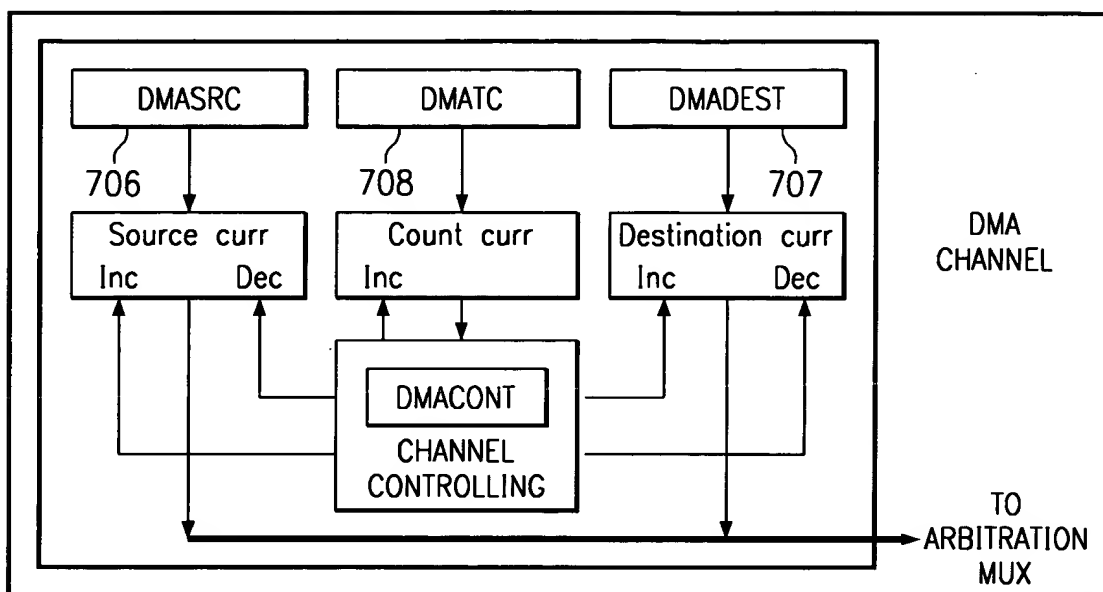
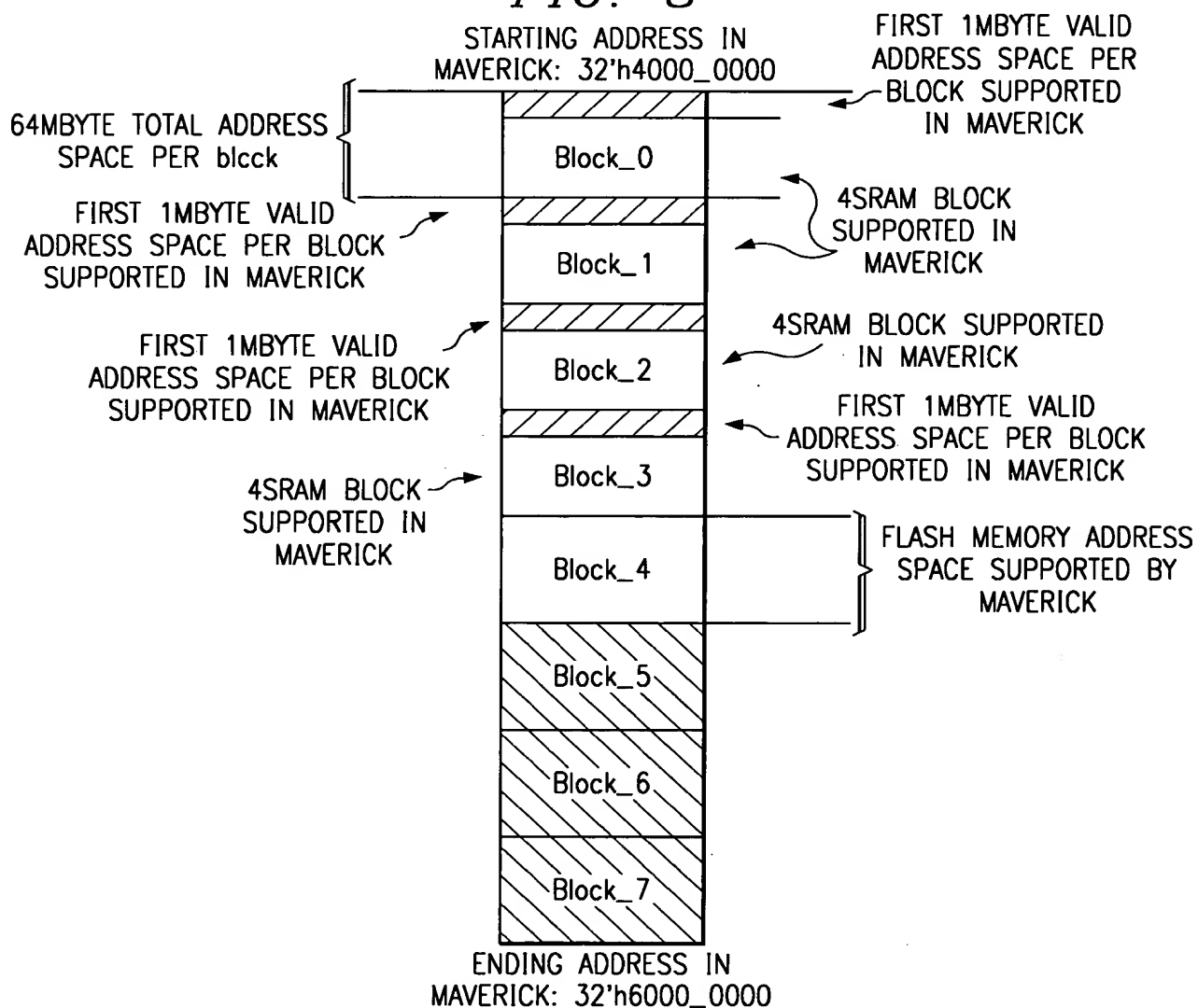


FIG. 8



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FIG. 9

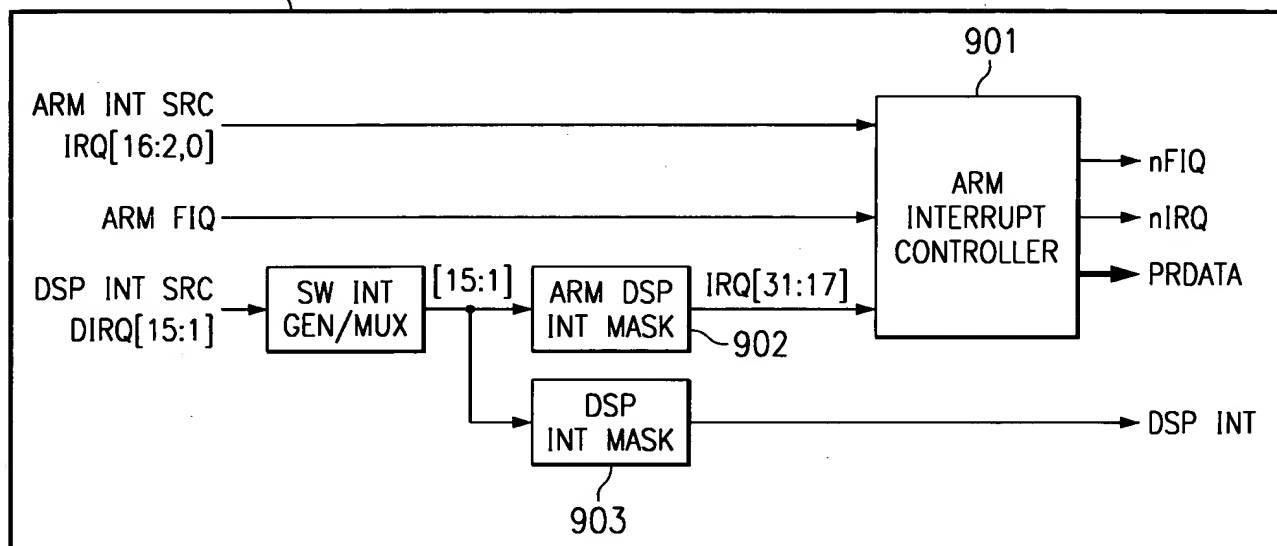
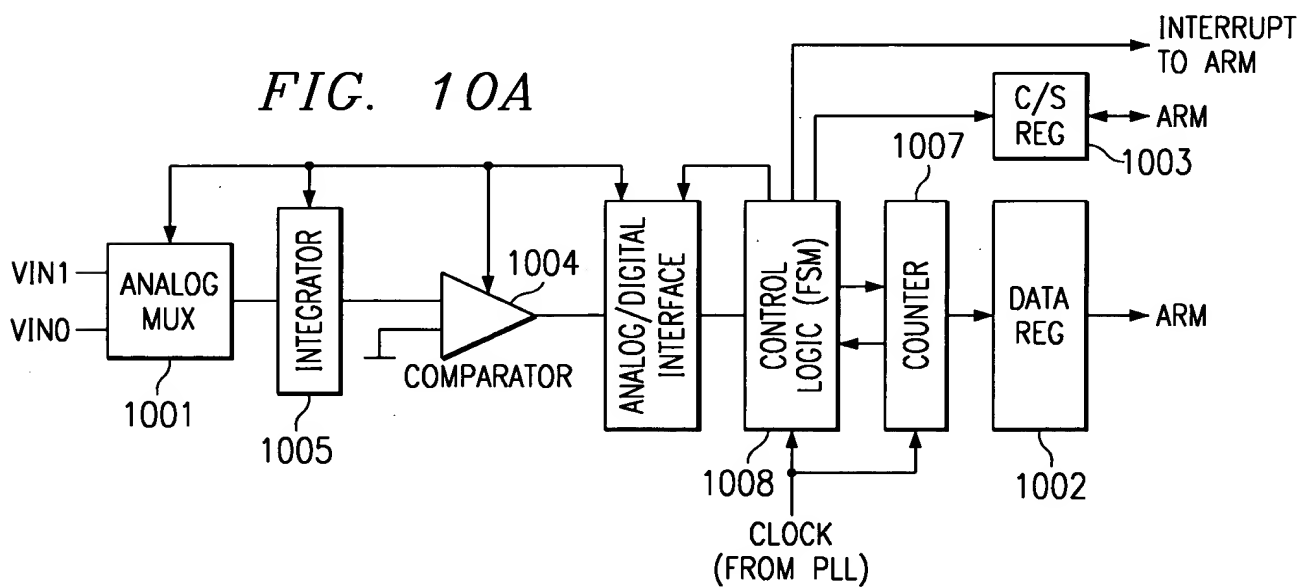


FIG. 10A



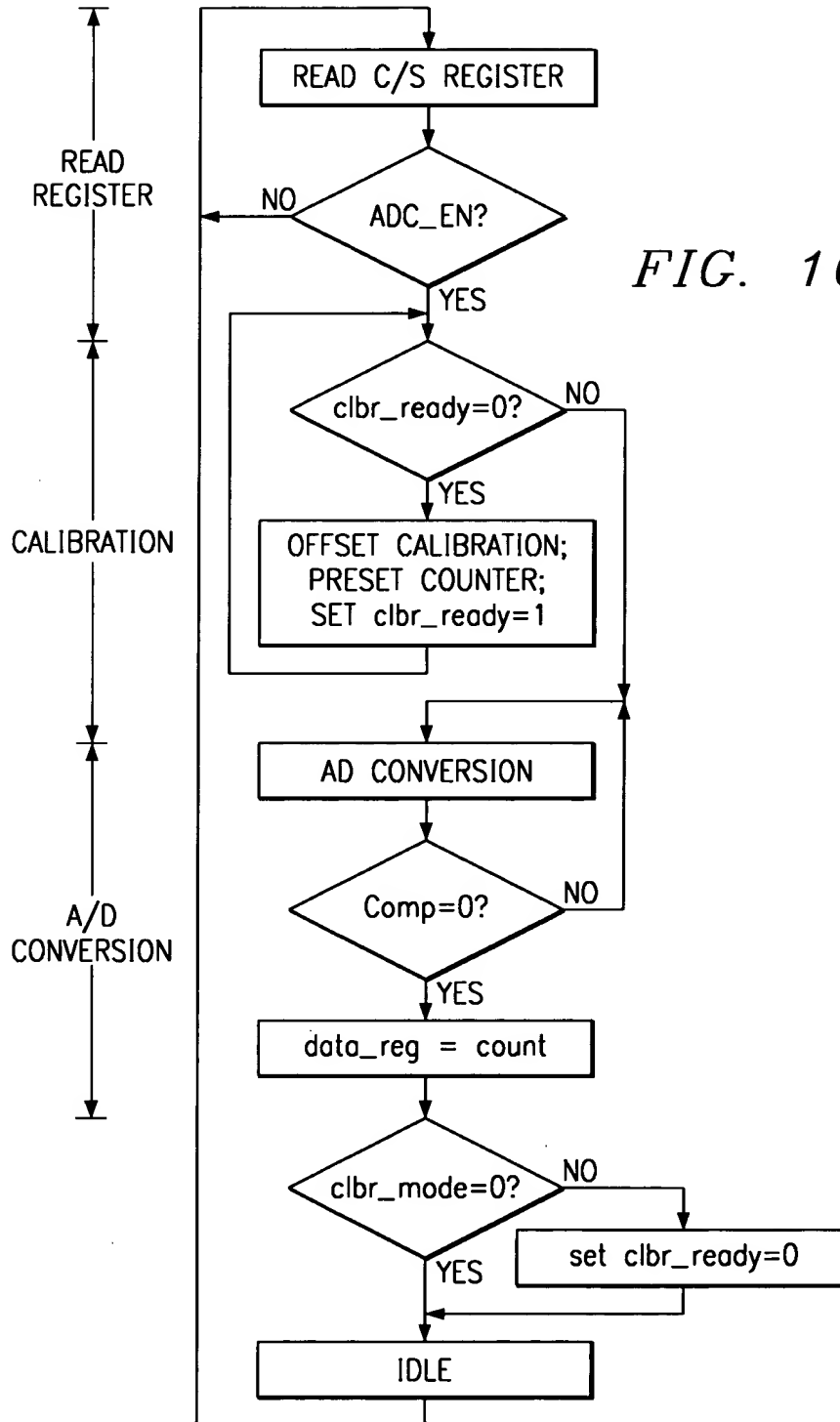


FIG. 11A

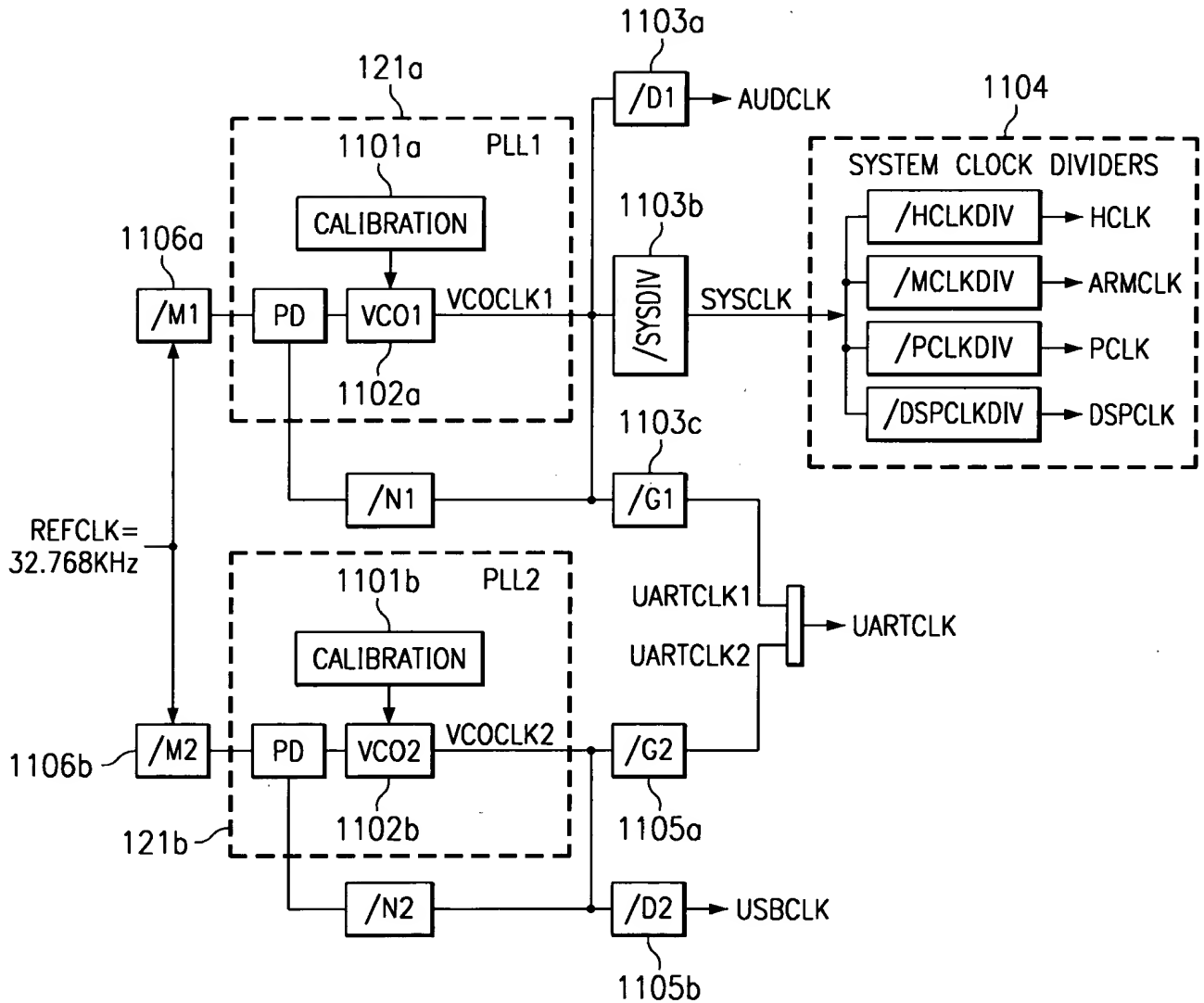
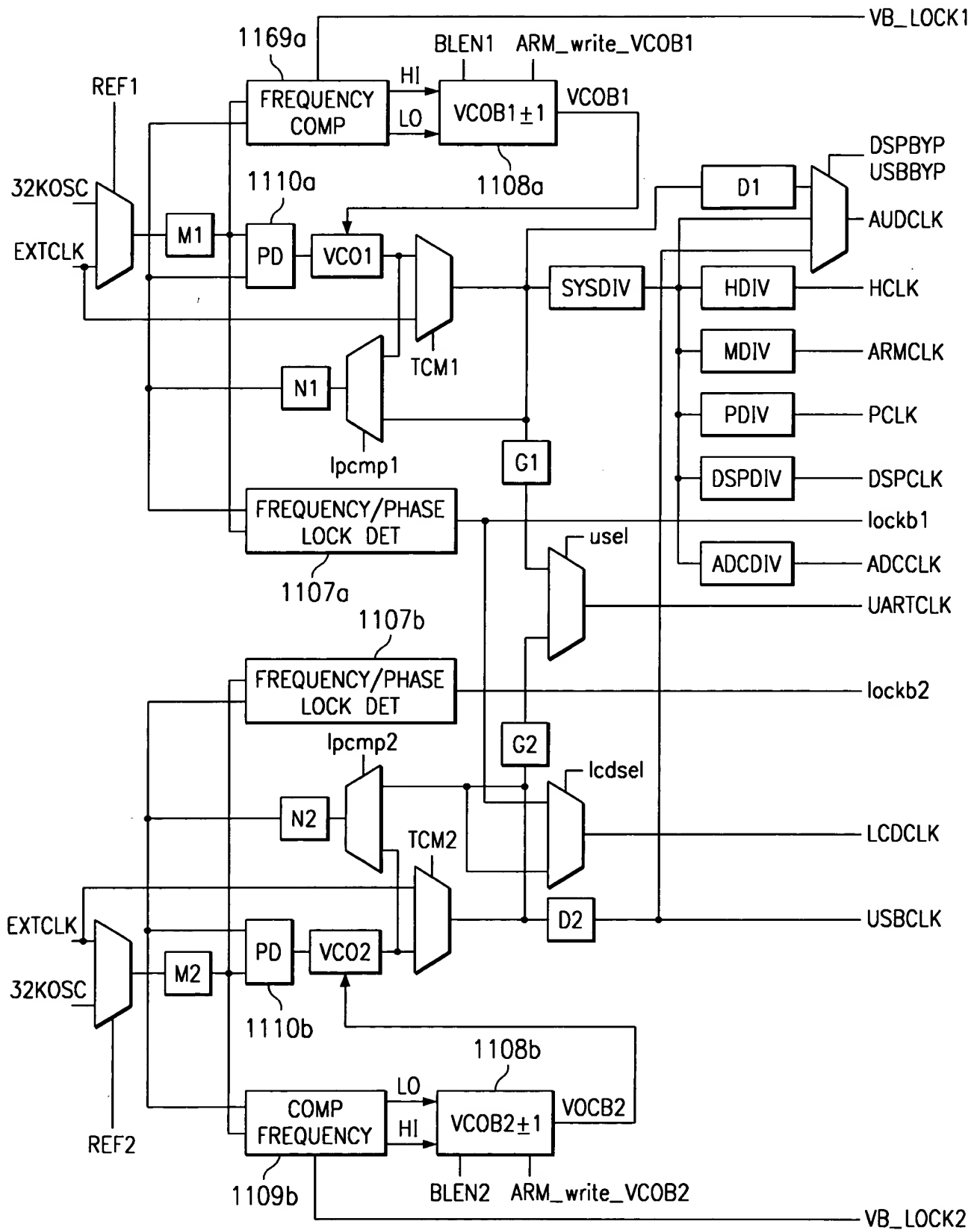


FIG. 11B



```

graph LR
    A[up_dn_diff FROM PD] --> B[COUNT DURING LOW PULSE]
    C[CLOCK FROM VCO] --> B
    B --> D[COMPARE WITH PHASE_LOCK_DS]
    D --> E[PHASE_LOCK]
  
```

```

graph LR
    M[FROM M DIVIDER] --> D128[/128/]
    D128 -- in_clk --> COUNTER1[COUNT THE NUMBER OF sample_clk DURING EVERY in_clk CYCLE]
    N[FROM N DIVIDER] -- sample_clk --> COUNTER1
    COUNTER1 --> COMPARE[COMPARE WITH FREQ LOCK_DS]
    COMPARE --> COUNTER2[TWO-WAY HYSTERESIS COUNTER]
    FREQ_LOCK_DS[FREQ_LOCK_DS] --> COUNTER2
    HYST_F_OUTLOCK[HYST_F_OUTLOCK] --> COUNTER2
    HYST_F_INLOCK[HYST_F_INLOCK] --> COUNTER2
    COUNTER2 --> FREQ_LOCK[FREQ_LOCK]
  
```

The diagram shows the EP7409 on the left and the SERIAL EEPROM on the right. The EP7409 has two pins labeled EEDAT and EECLK. The SERIAL EEPROM has two pins labeled SDA and SCL. A pull-up resistor connects the +3.3V supply to the SDA pin. The EEDAT pin is connected to the SDA pin. The EECLK pin is connected to the SCL pin. Both the EP7409 and the SERIAL EEPROM are connected to a +3.3V supply and ground.

G. 12B

CLOCK LOW 4.7us, CLOCK HIGH 4.0us, t_R 1000ns, 4.7us, 4.0ns, 0ns, 250ns, 4us, STOP SETUP, DATA IN, START SETUP, START HOLD, DATA HOLD, DATA, DATA OUT, 3.5us, t_F 300ns

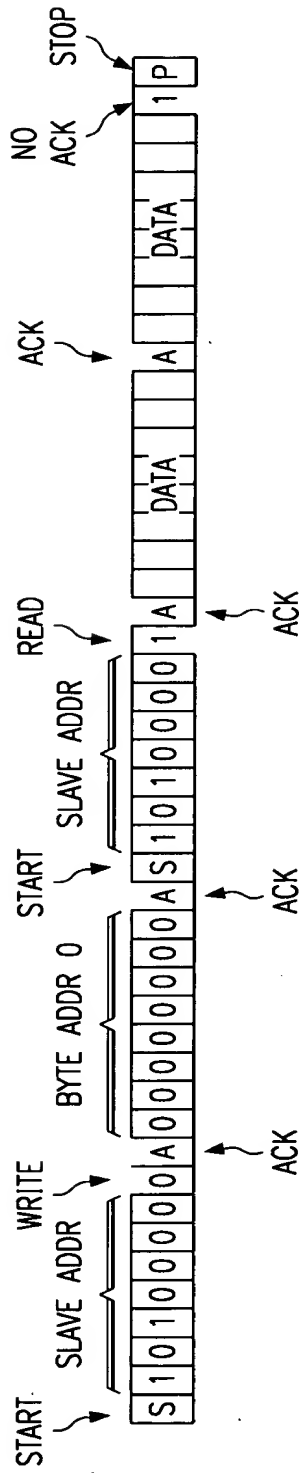
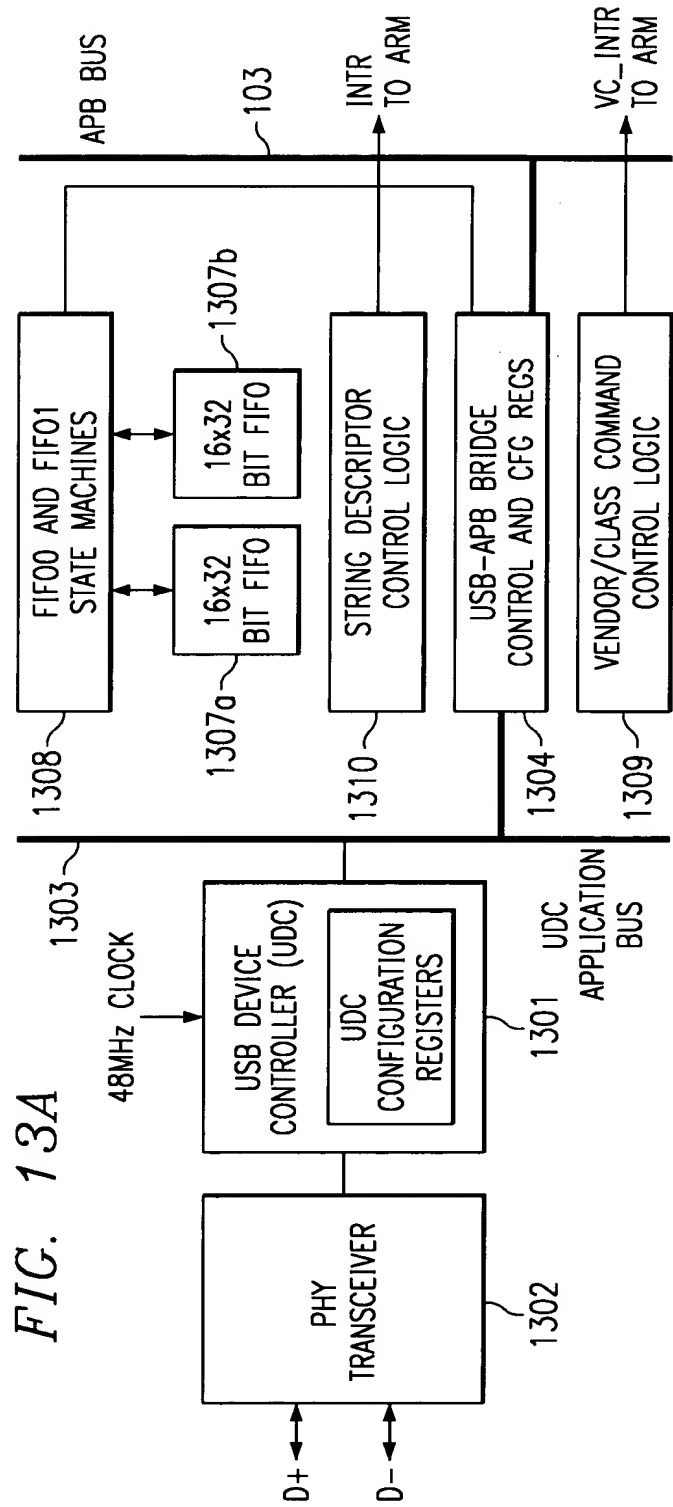


FIG. 12C

FIG. 13A



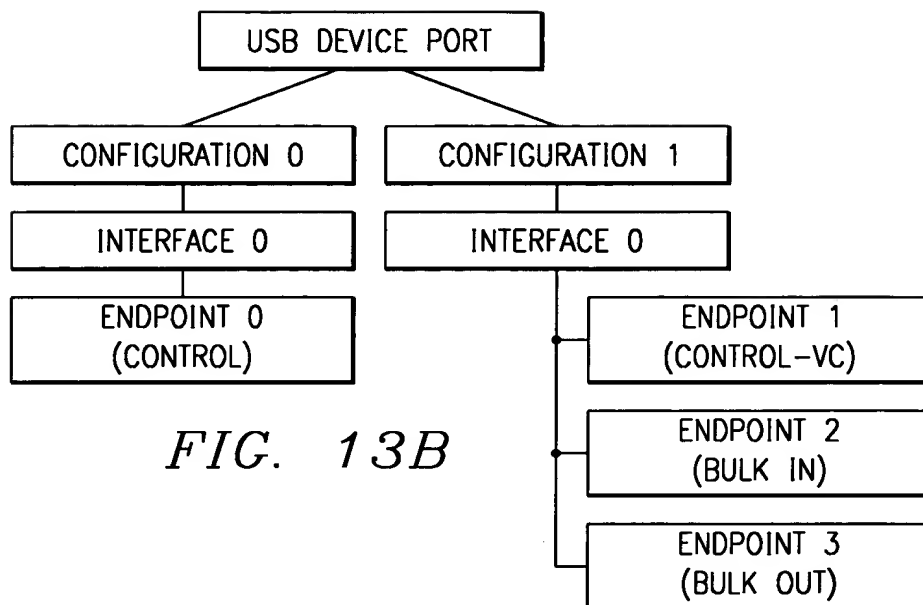


FIG. 13B

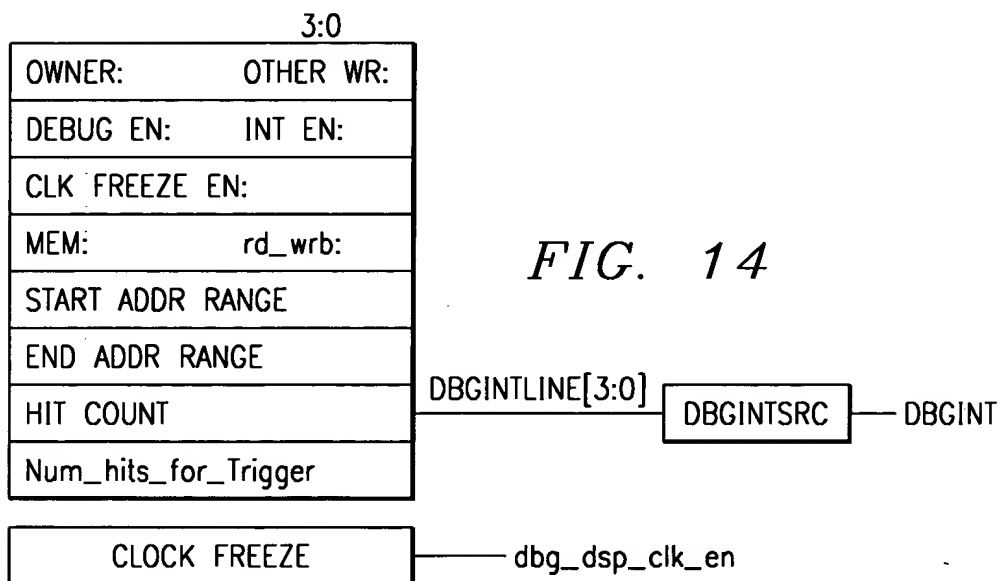


FIG. 14

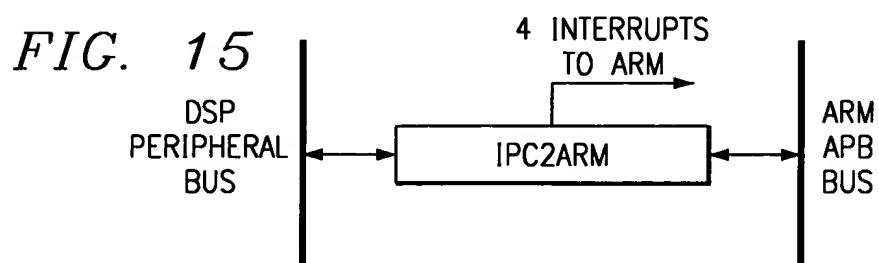


FIG. 15

FIG. 16A

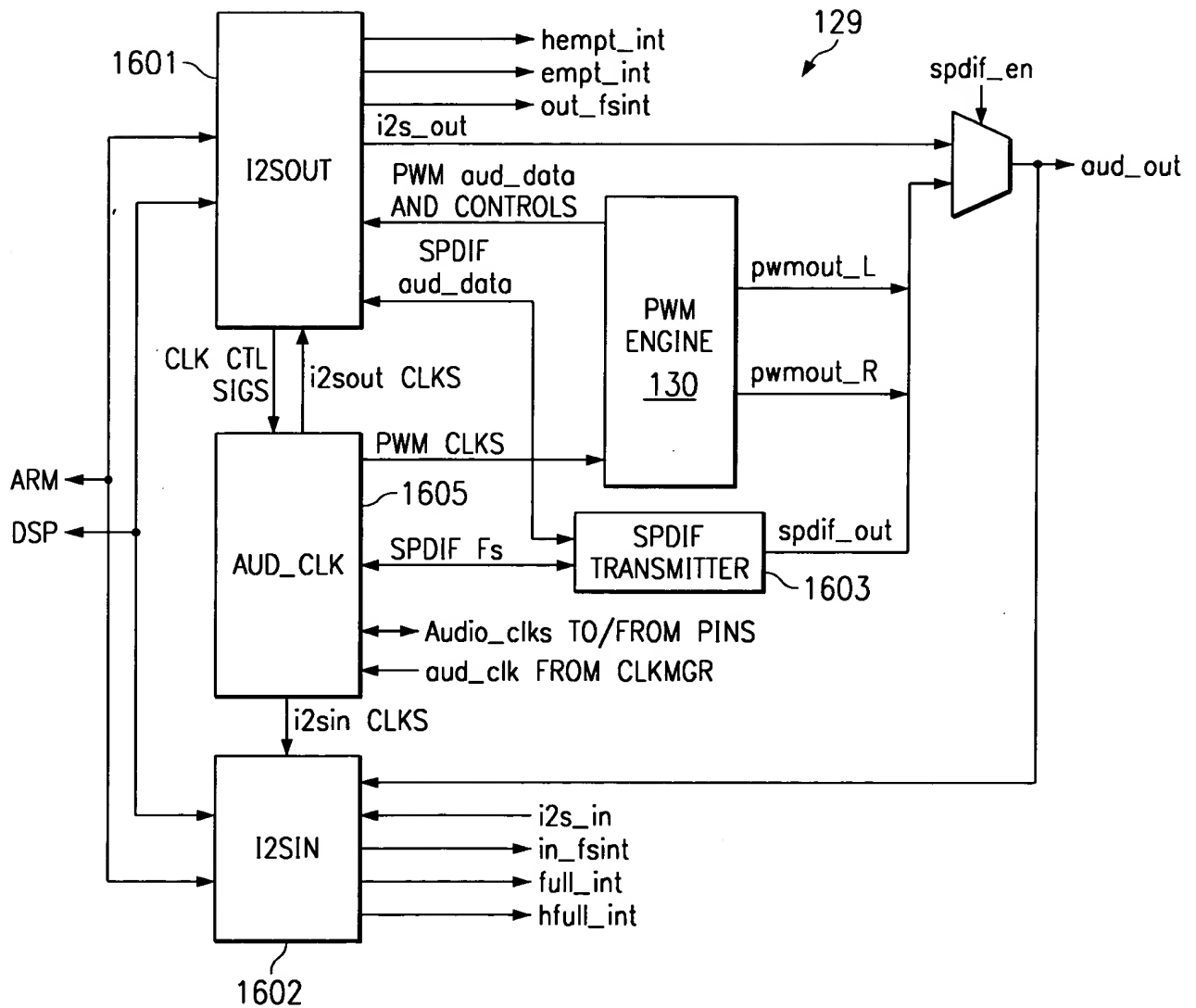


FIG. 16B

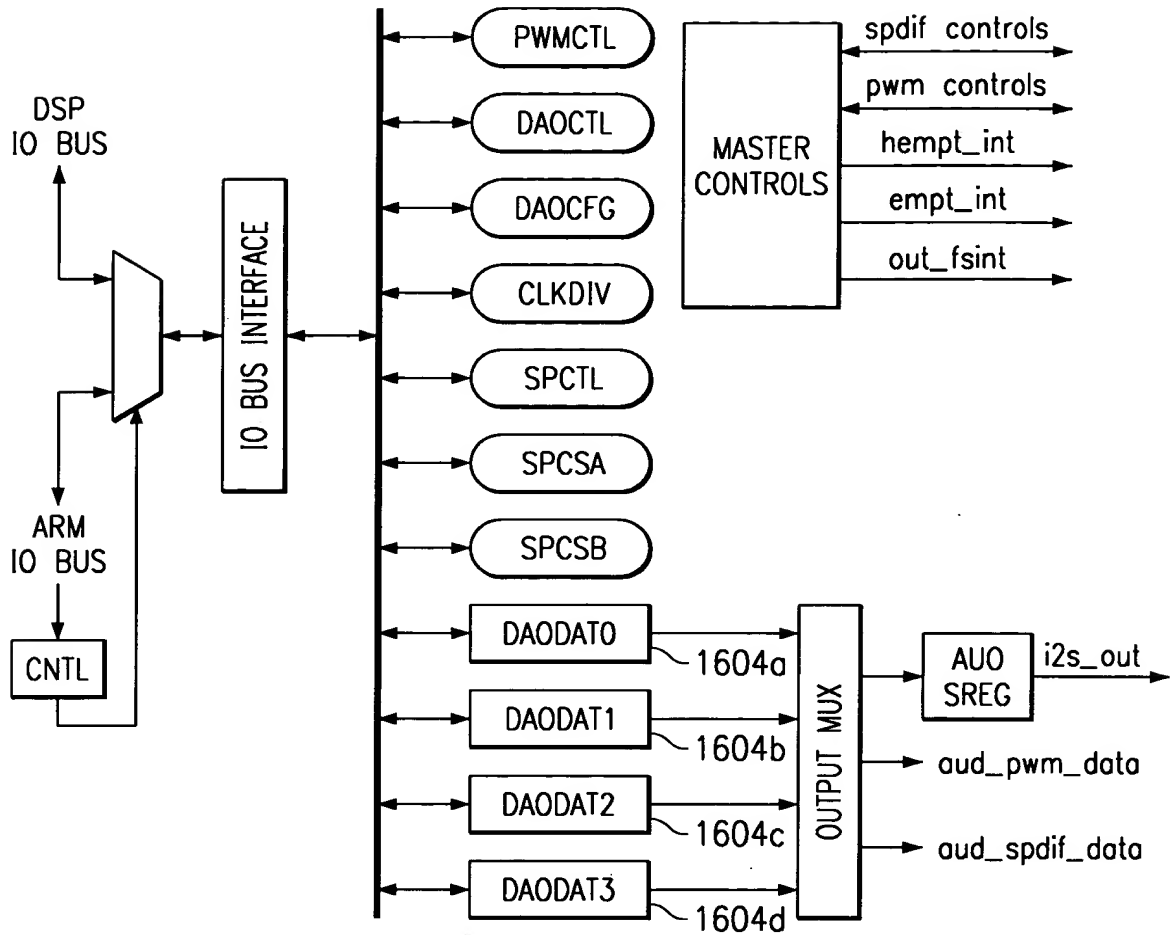


FIG. 16C

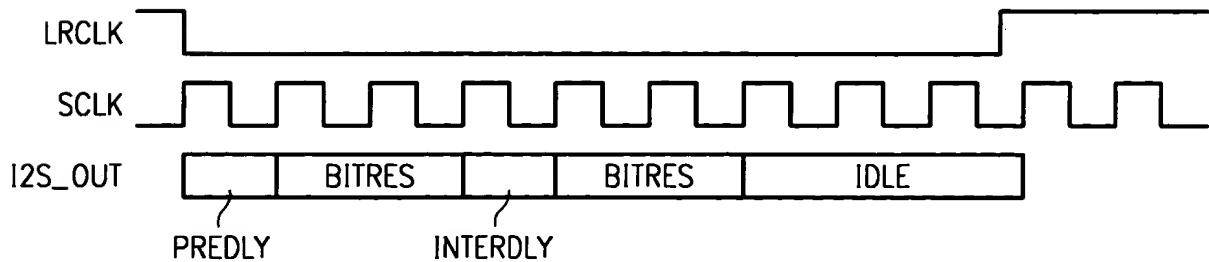


FIG. 16D

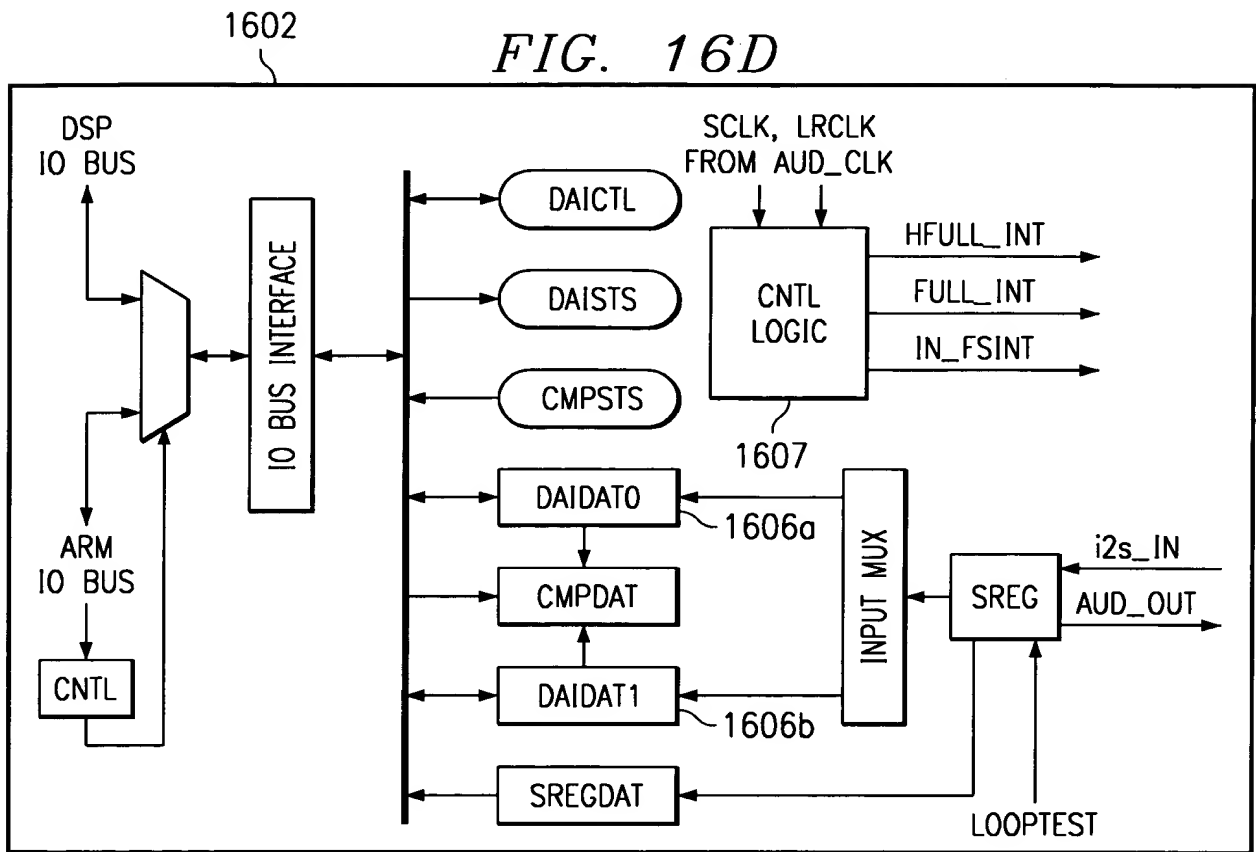


FIG. 19A

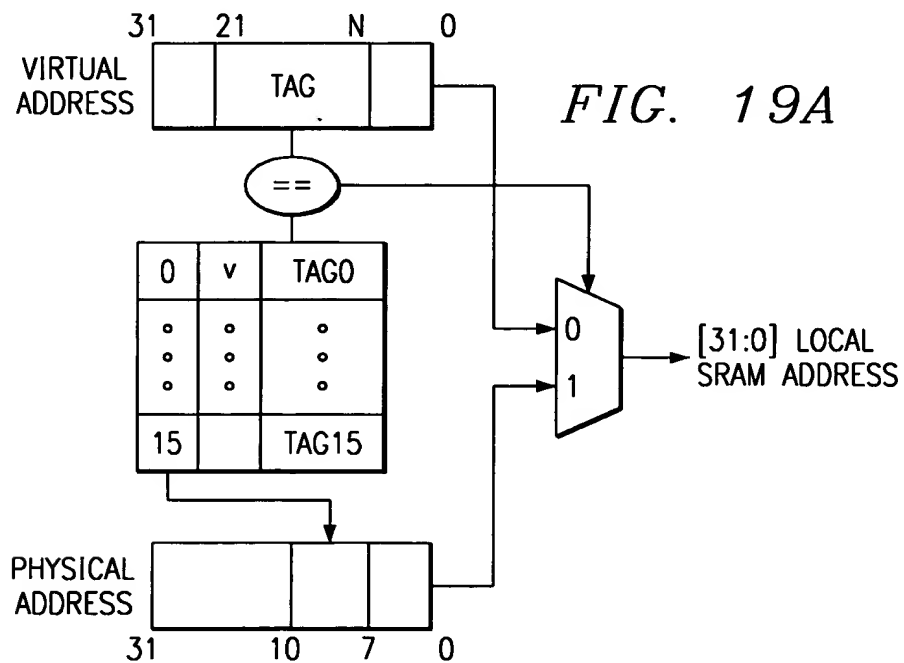


FIG. 19B

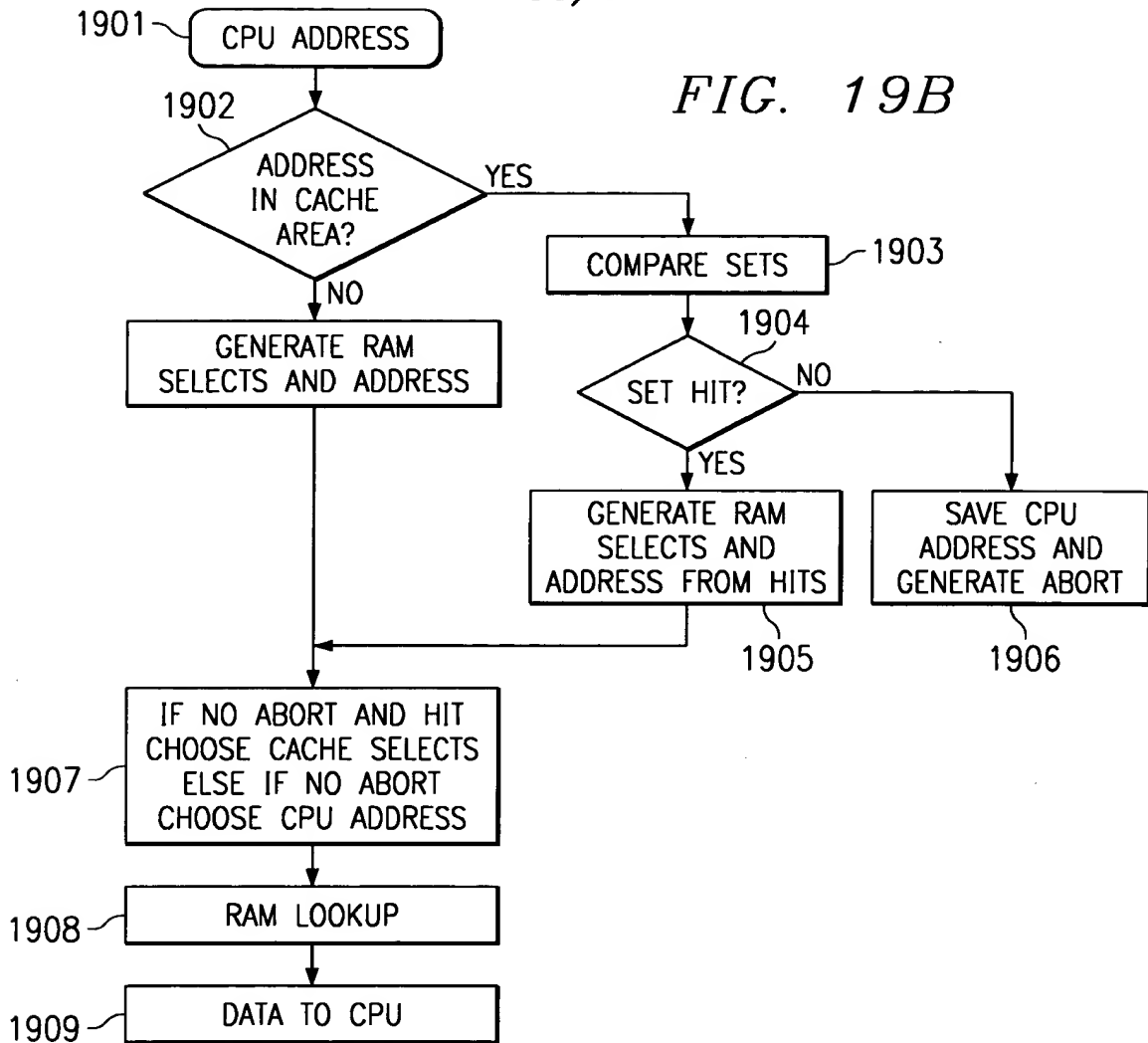
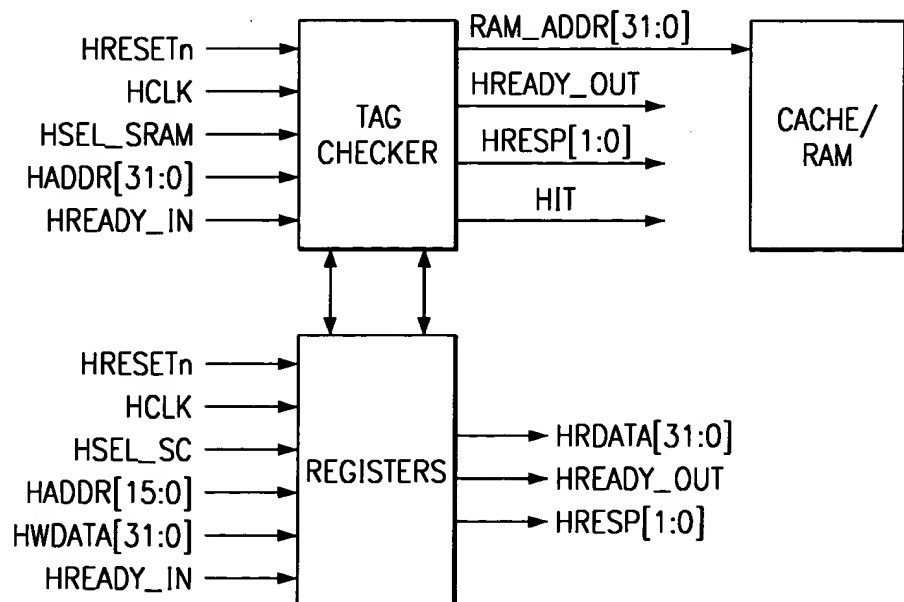


FIG. 19C



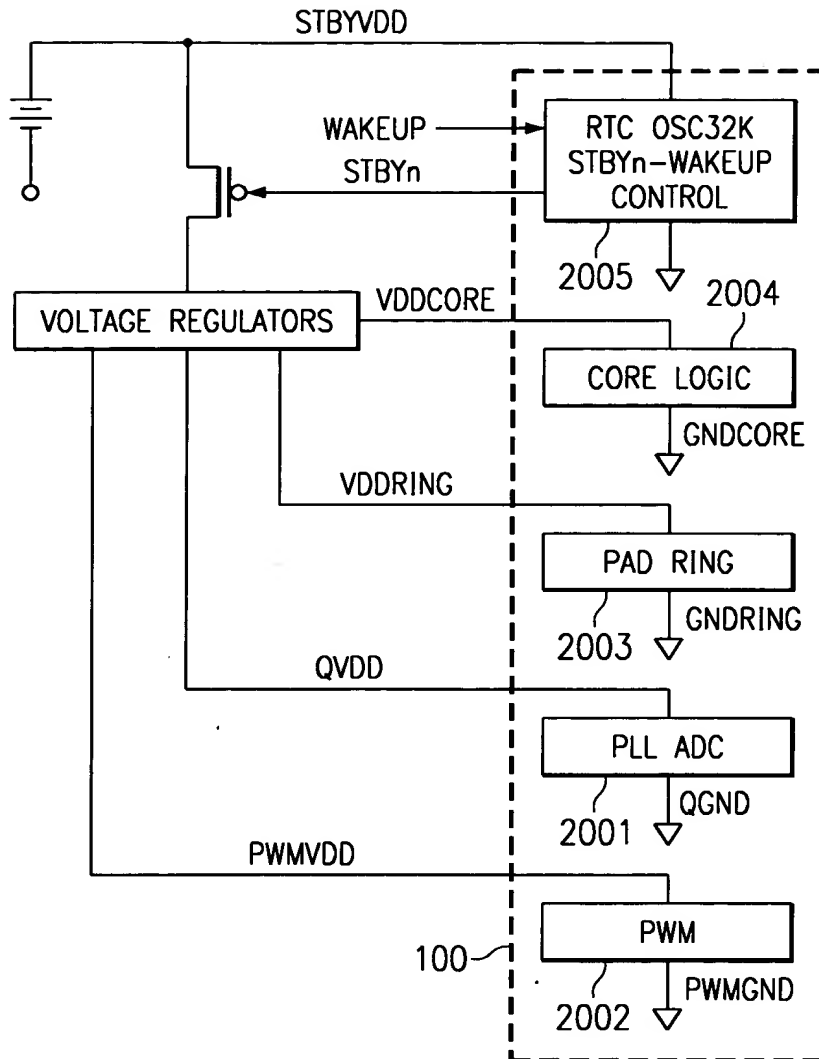


FIG. 20A

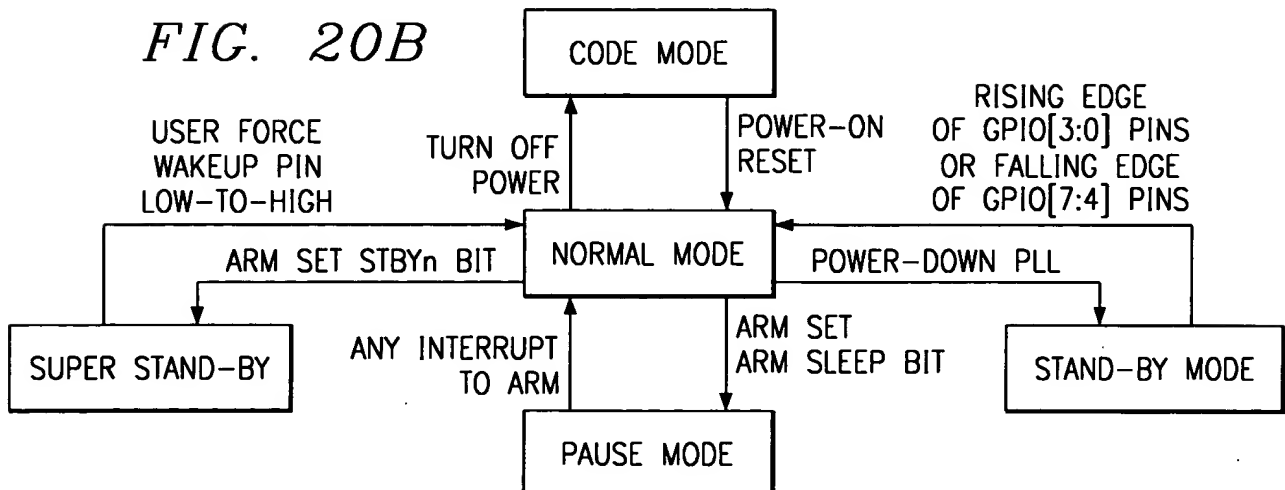


FIG. 20B

FIG. 20C

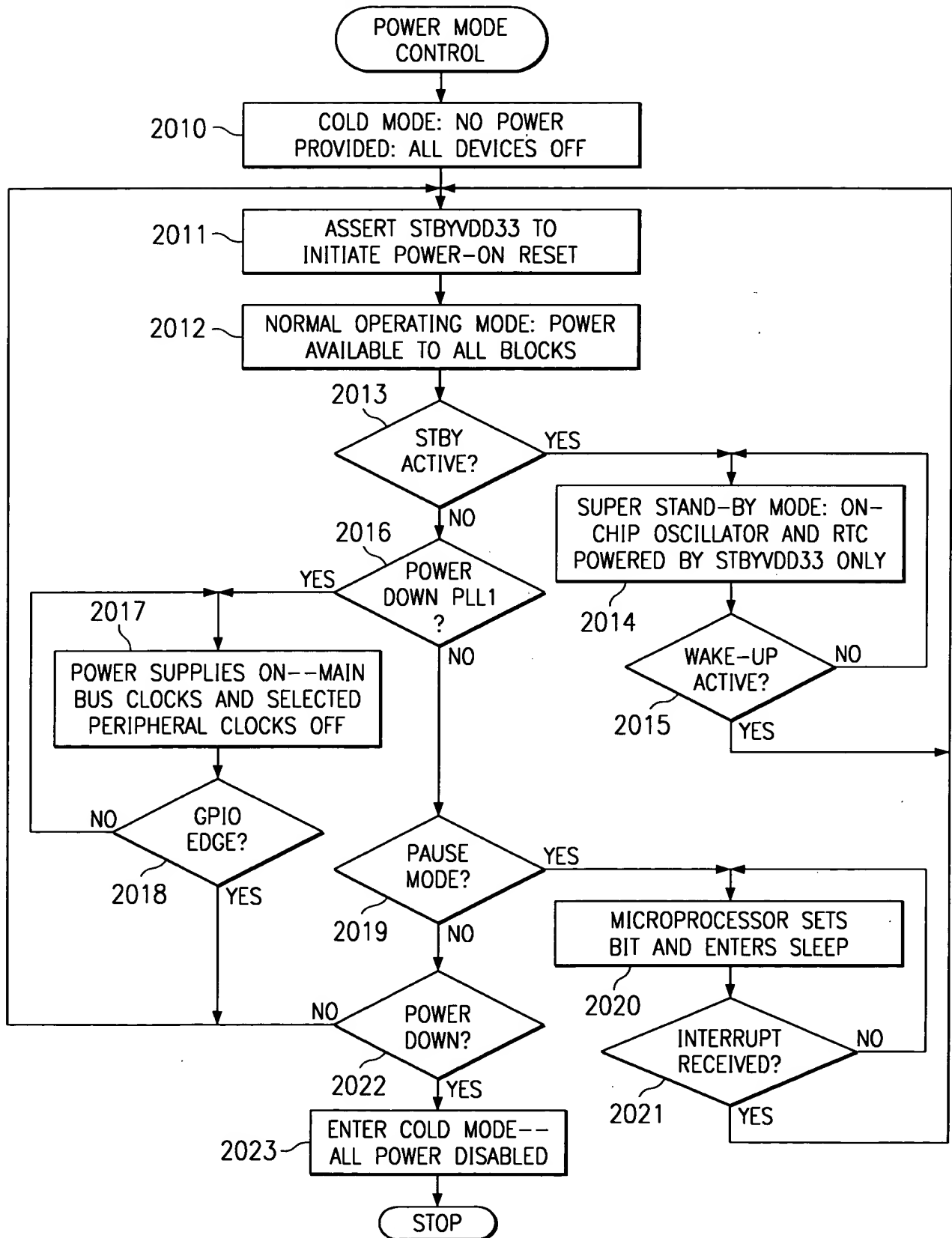
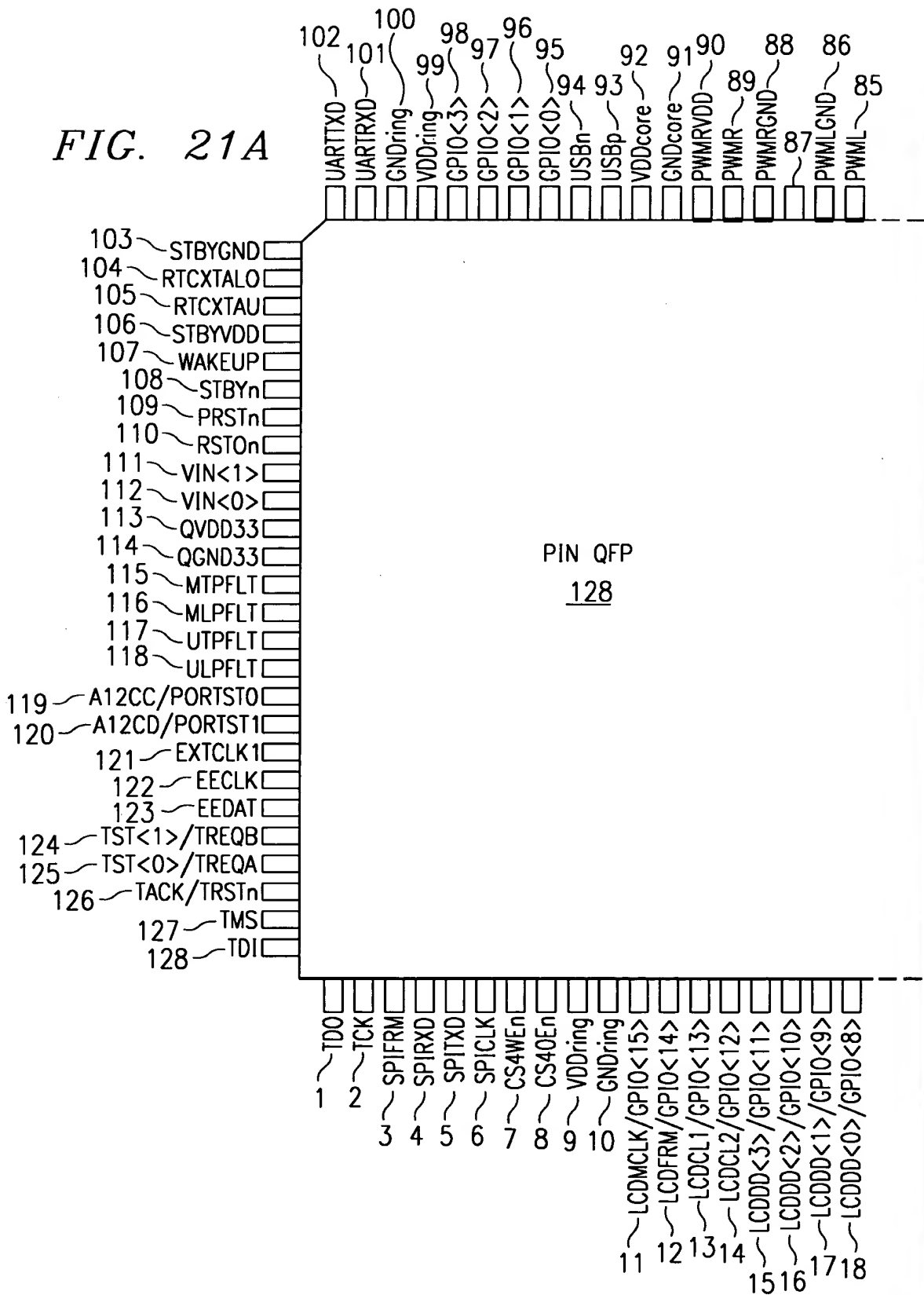


FIG. 21A

TO
FIG.
21B

T00T60" 460T6600

FROM
FIG.
21APIN QFP
128

FIG. 21B

